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NEC:LunarEagle

MSI:MS-7420N1

Version:0D



CPU: Conroe family processors /WolfDale/Yorkfield in LGA775 Package.

System Chipset:

Intel EagleLake-Q+Intel ICH10-DO

On Board Device:

BIOS -- SPI Flash 32M

LAN --INTEL 82567LM Boazman

Super I/O -- SMSC5617C

AUDIO -- Realtek HD ALC262VD

Clock GEN-IDTCV184-2

TPM-SLB 9635 TT1.2

Main Memory:

Due-channel DDR-III * 2 (1066MHZ)

Intersil PWM:


Controller: Intersil ISL6334 (3 Phases)

Expansion Slots:

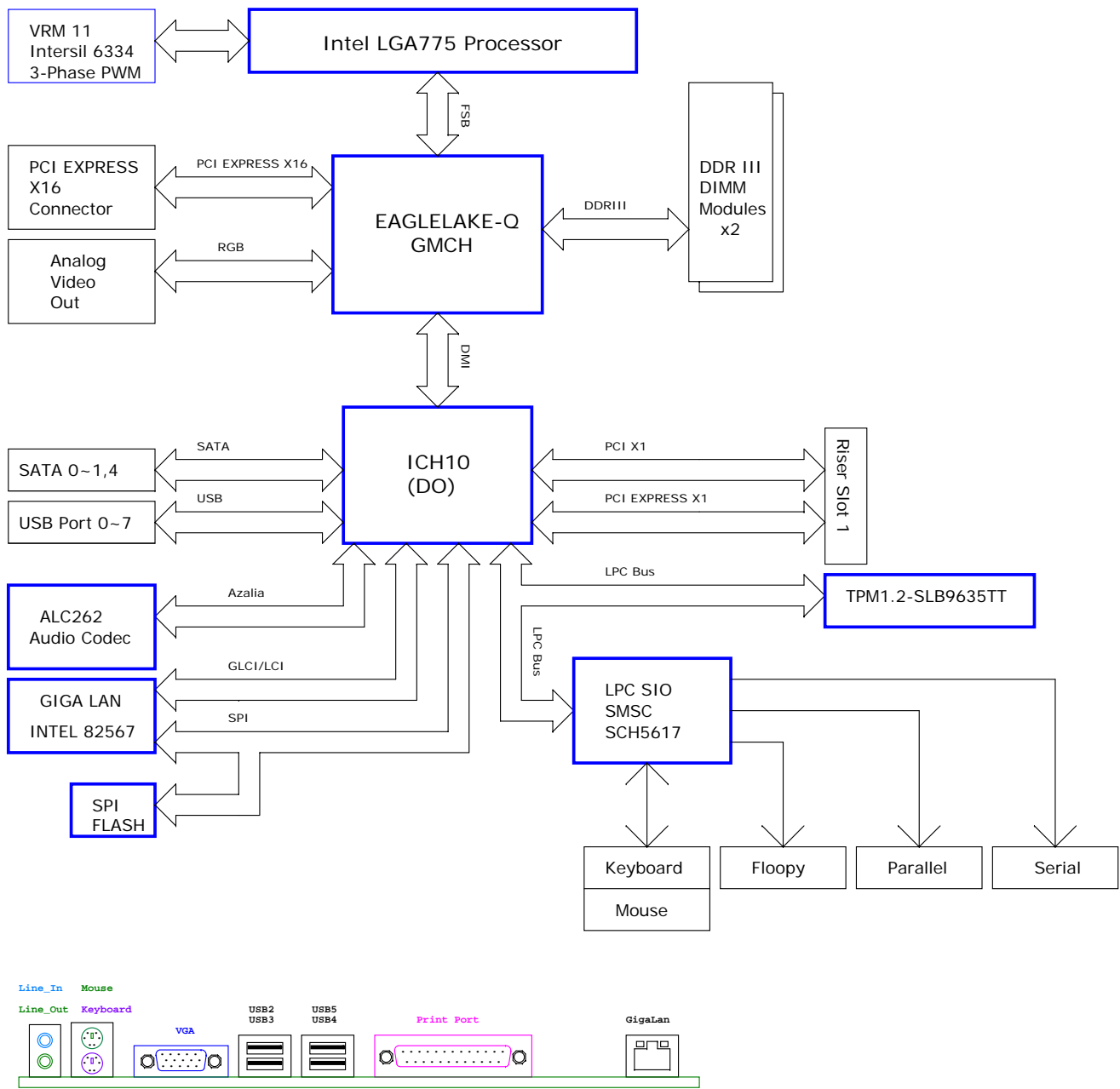
PCI-E(X16) Slot *1

Riser Slot :(PCIx1/PCI-E(x1)x1)

MS-6497N1	ERP Number	Function
MS-7420-0C	601-7420-C10	Mainboard
MS-4046-2A	604-4046-020	Power Button/LED board
MS-4085-10	604-4085-030	Front Audio Board
MS-4048-41	604-4048-050	Front USB Board
MS-4121-10	604-4121-010	Riser Card

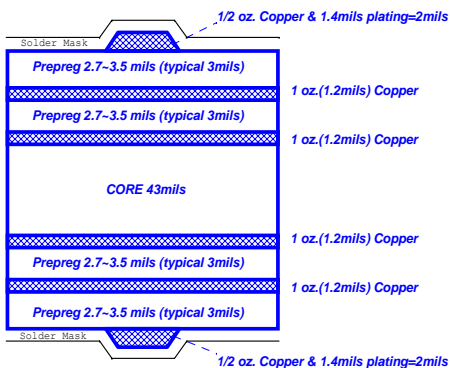
 MICRO-START INT'L CO.,LTD.		
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Block Diagram



Board Stack-up (6 layers)

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
Differential Clock : 18/4/10/4/18

Example Fab Drawing Note (1080 Prepreg PCB)


Trace Width (mils)	Differential Spacing (mils)	Target Impedance	Tolerance
4.0	NA	50-ohm, single-ended	15%
6.5	NA	40-ohm, single-ended	15%
7.5	NA	30-ohm, single-ended	15%
9.5	NA	32-ohm, single-ended	15%
3.9	8.1	95-ohm, differential	20%, reference only
4.5	7.5	90-ohm, differential	20%, reference only

Eaglelake(GMCH) Impedance Requirements by Interface

Interface	Impedance Required
FSB (All)	4x signals 42-ohm, others 50-ohm, single-ended
Controller Link	50-ohm, single-ended
DDR2 (DQ, DQS, DM, CLK, CLK#)	40-ohm, single-ended
DDR2 (Control)	43-ohm, single-ended
DDR2 (Command)	33-ohm, single-ended
DDR3 (CLK, CLK#)	36-ohm, single-ended
DDR3 (DQ, DQS, DM)	20/37-ohm, single-ended
DDR3 (Control)	36-ohm, single-ended
DDR3 (Command)	32-ohm, single-ended
PCI Express, DMI	95-ohm, differential
VGA	97-ohm, single-ended at MCH breakout, then 50-ohm, single-ended to VGA connector

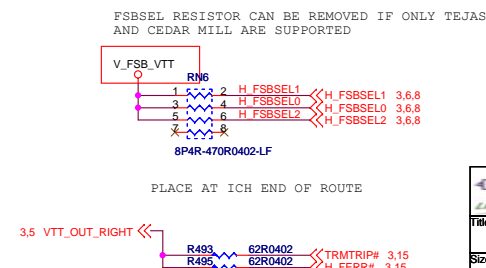
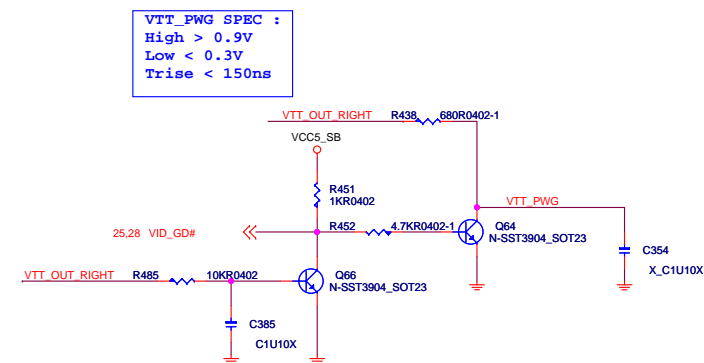
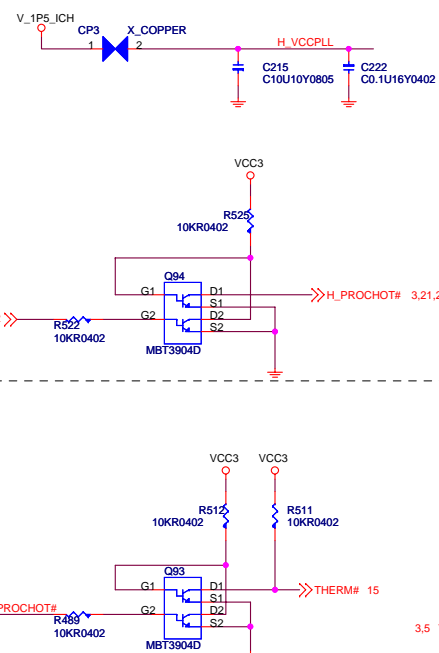
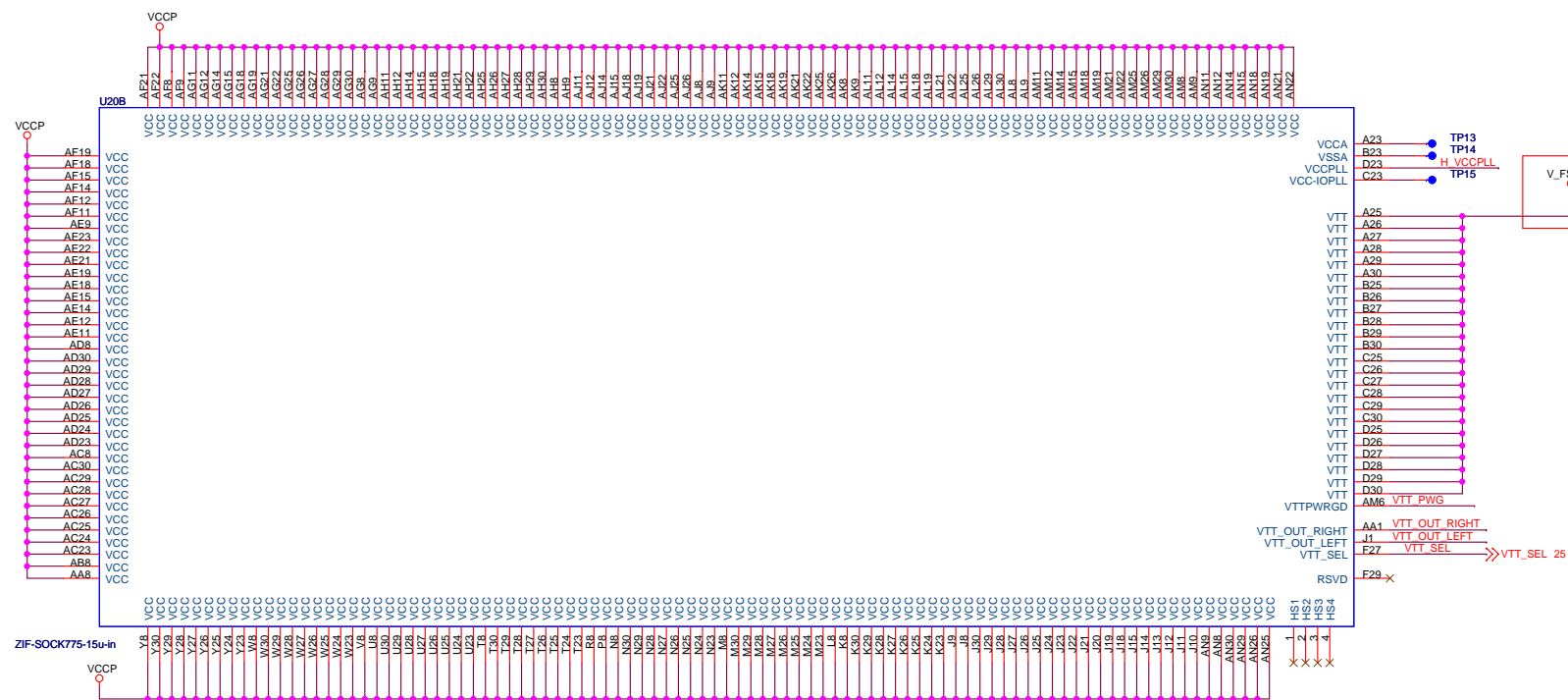
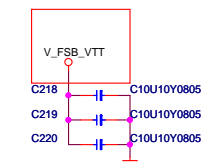
ICH10 Impedance Requirements by Interface

Interface	Impedance Required
PCI	50-ohm, single-ended
Controller Link	50-ohm, single-ended
Miscellaneous	50-ohm, single-ended
PCI Express, DMI	95-ohm, differential
SATA	95-ohm, differential
USB	90-ohm, differential

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[illegible]

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)

BIOS wirters Guide
PDG:page109

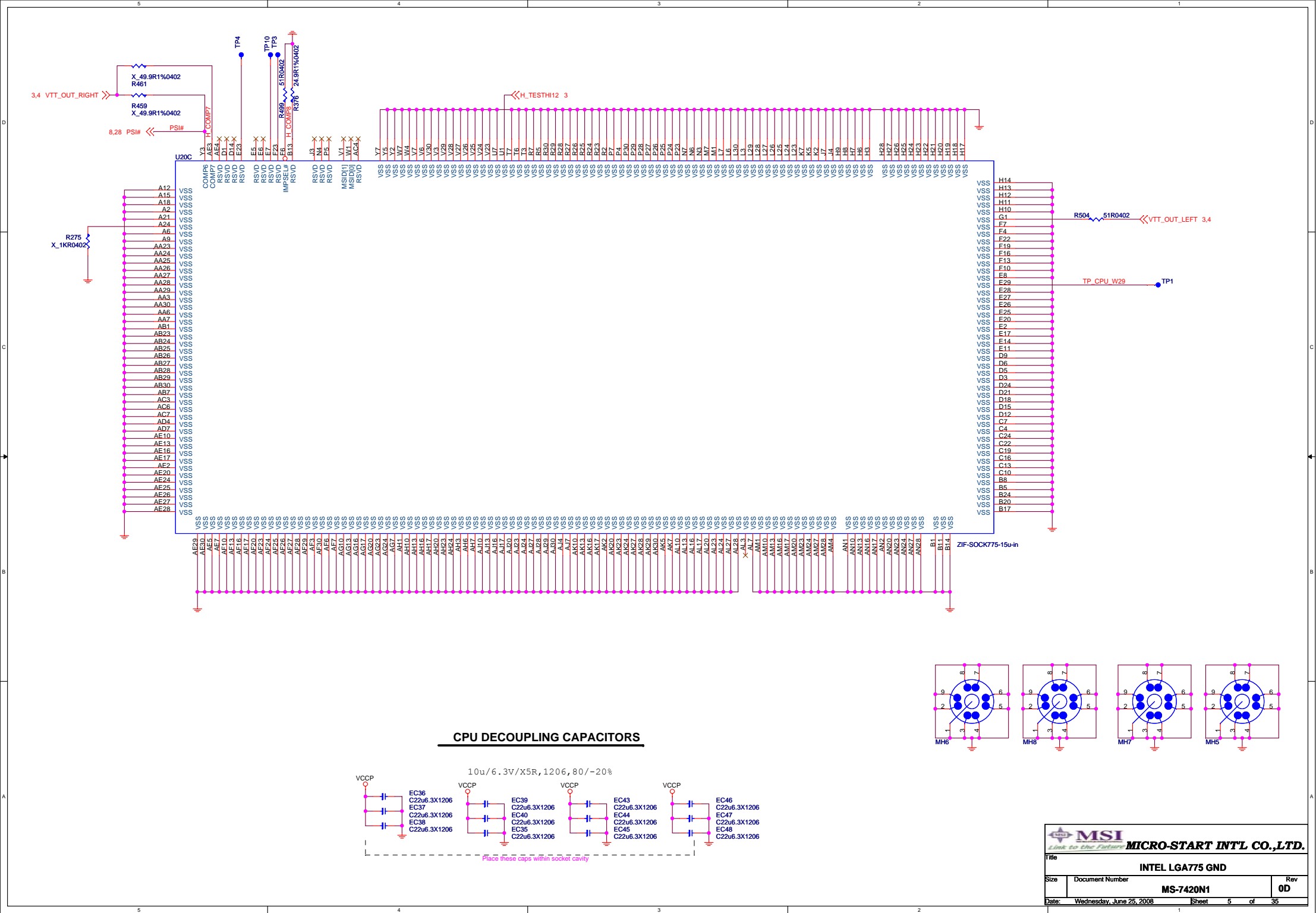
CAPS FOR FSB GENERIC

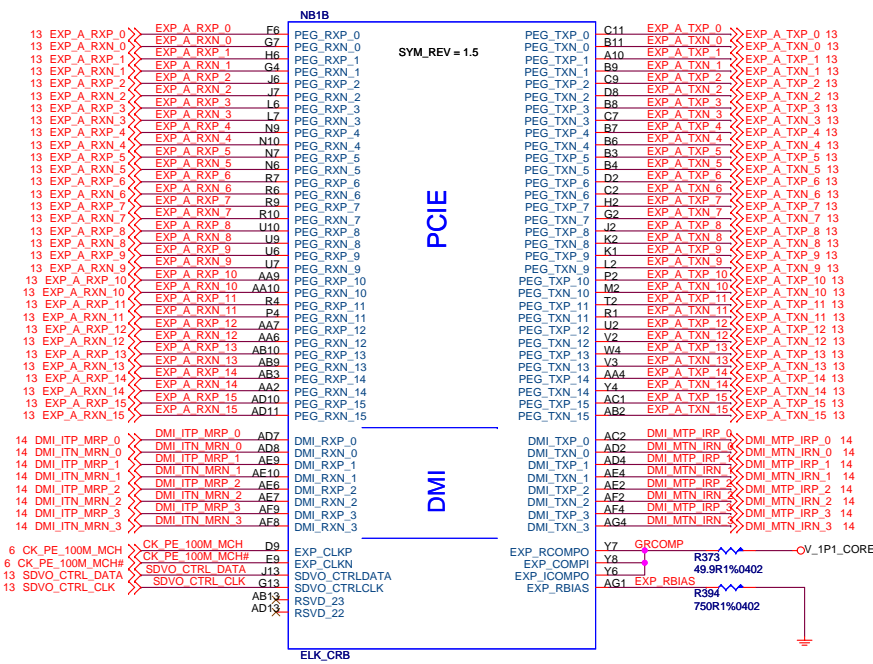
```
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
```

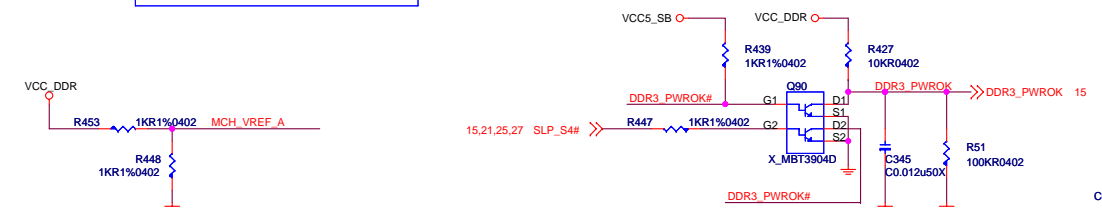
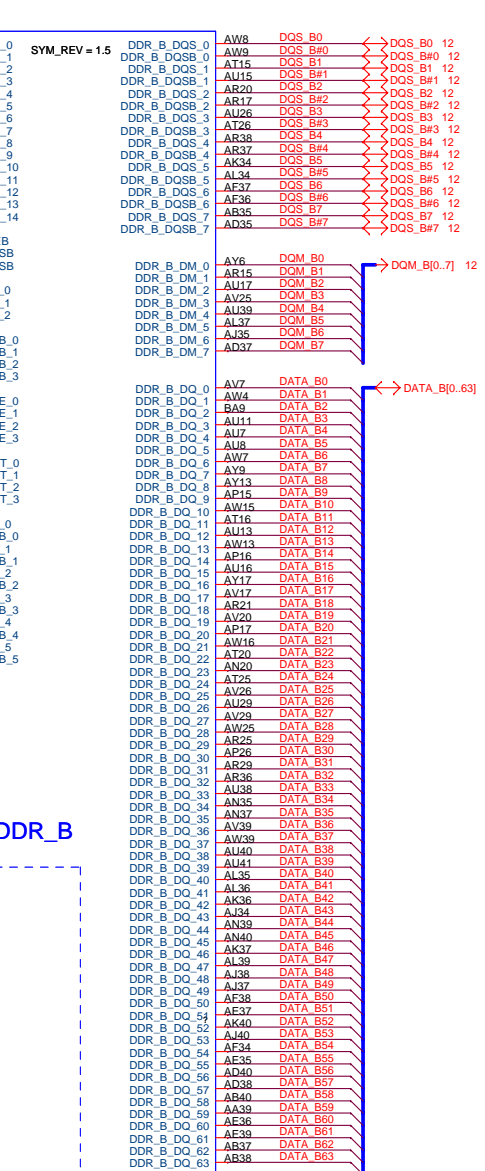
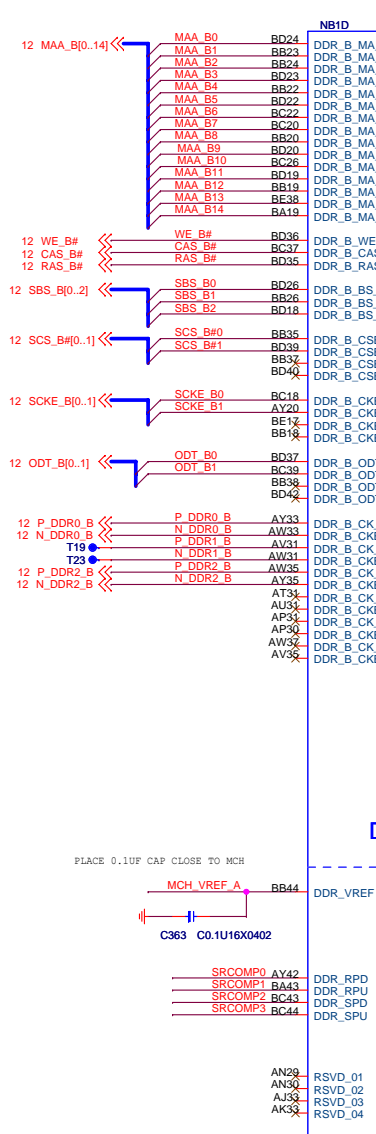
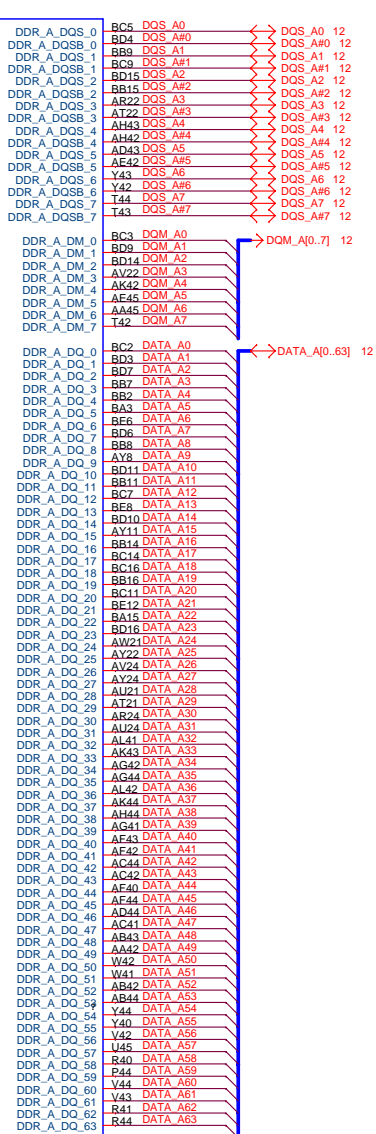
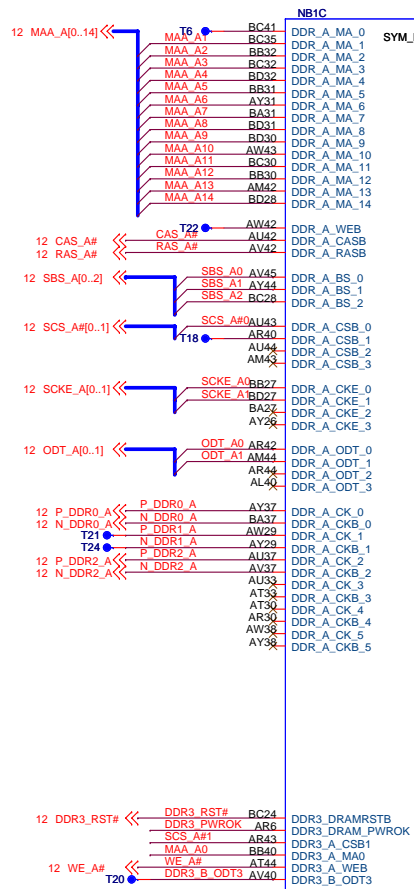
GP1018	GP1028	Rasio sel
1	1	0,67
1	0	0,65
0	1	0,63
0	0	0,615

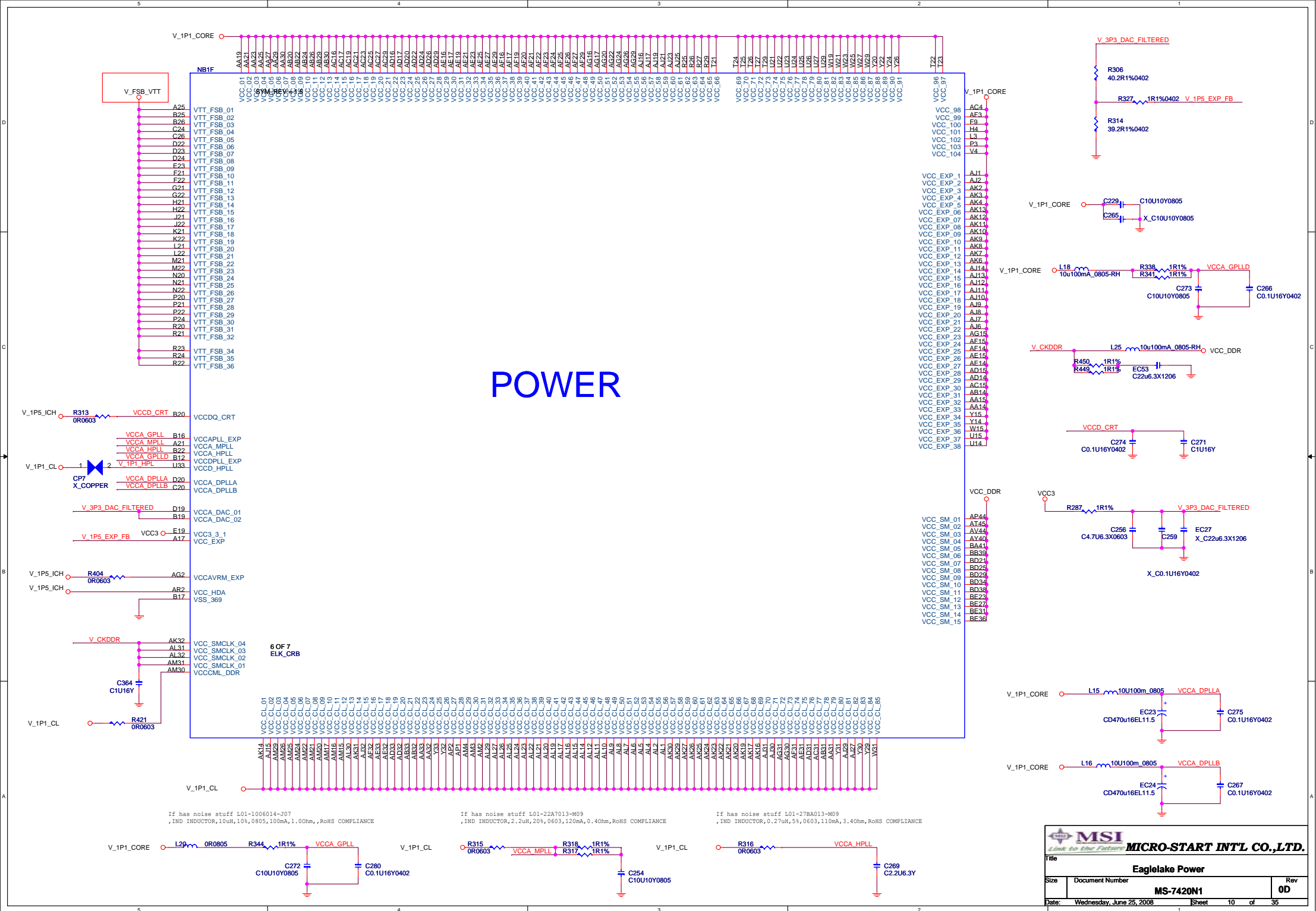
PLACE AT CPU END OF ROUTE

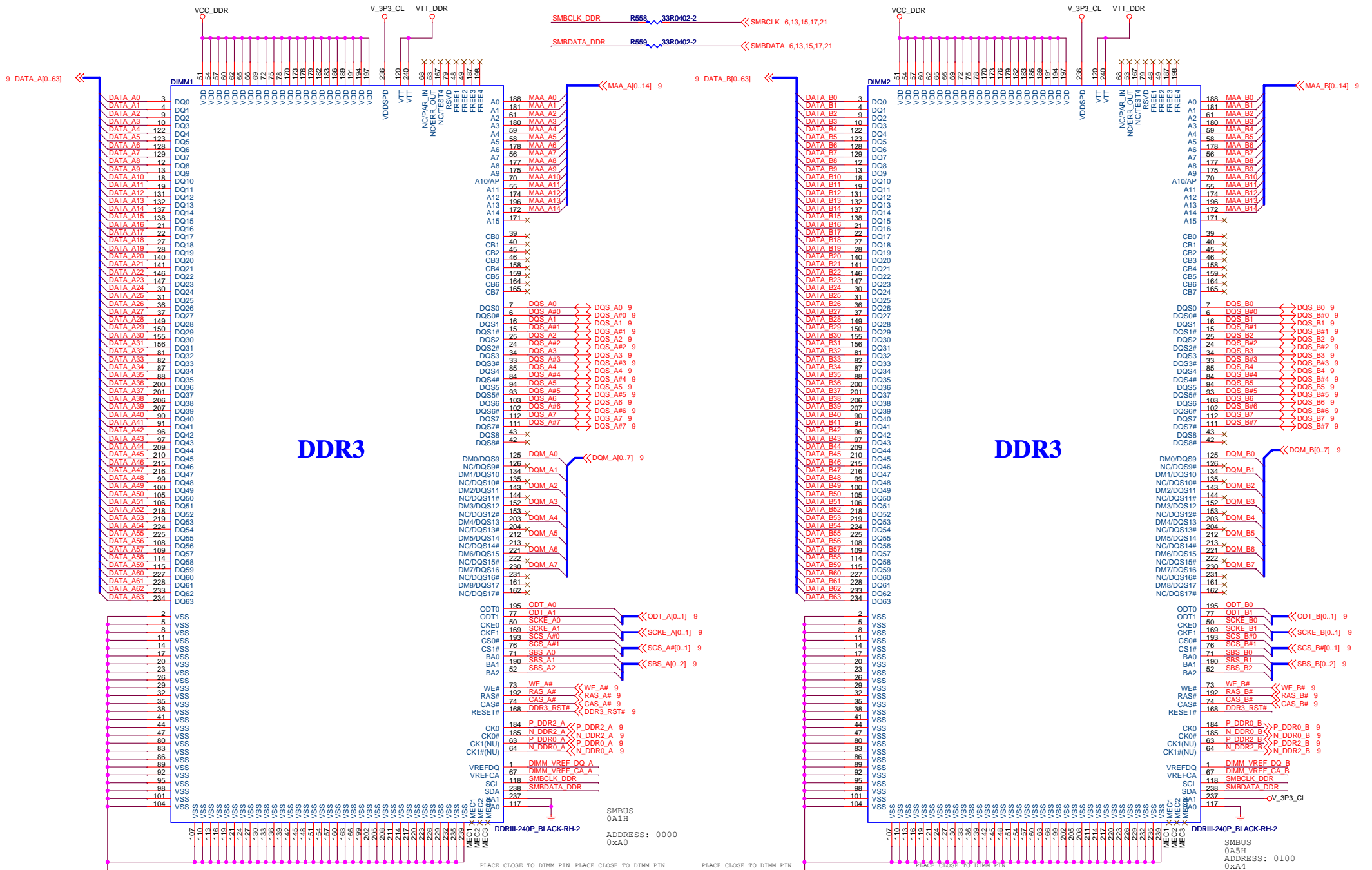
PLACE AT ICH END OF ROUTE

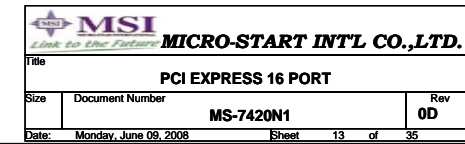


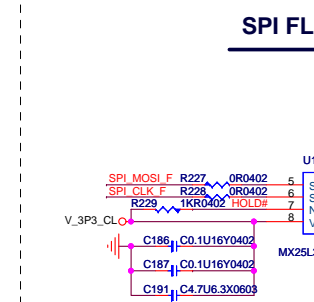
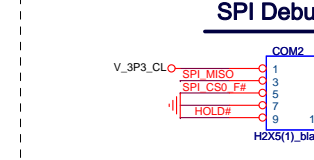
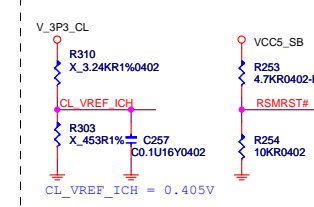
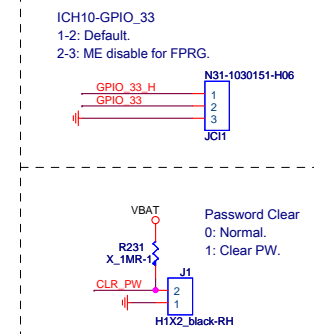
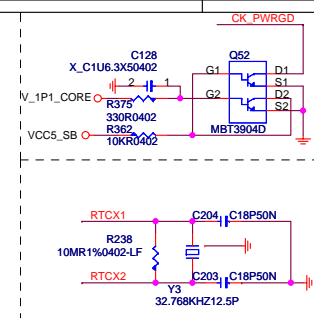
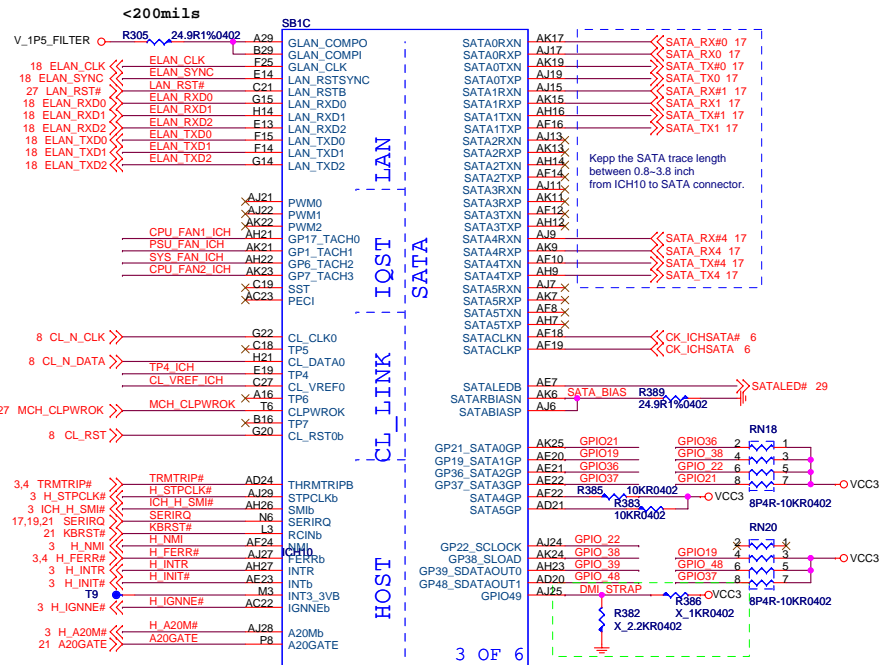






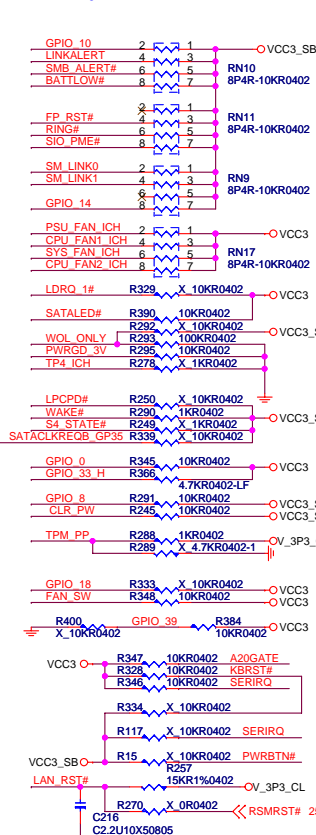




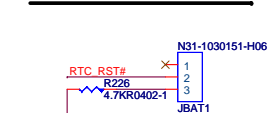


ICH10 PULL-UP RESISTORS

ALL COMPONENTS CLOSE TO ICH10
Trace length is less than 3inches to ICH10.

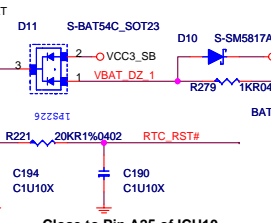


CLEAR CMOS JUMPER

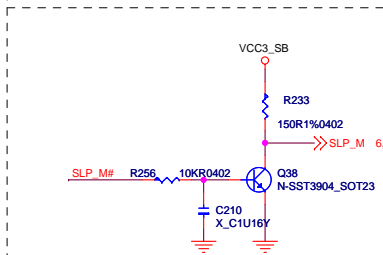
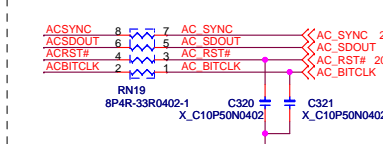
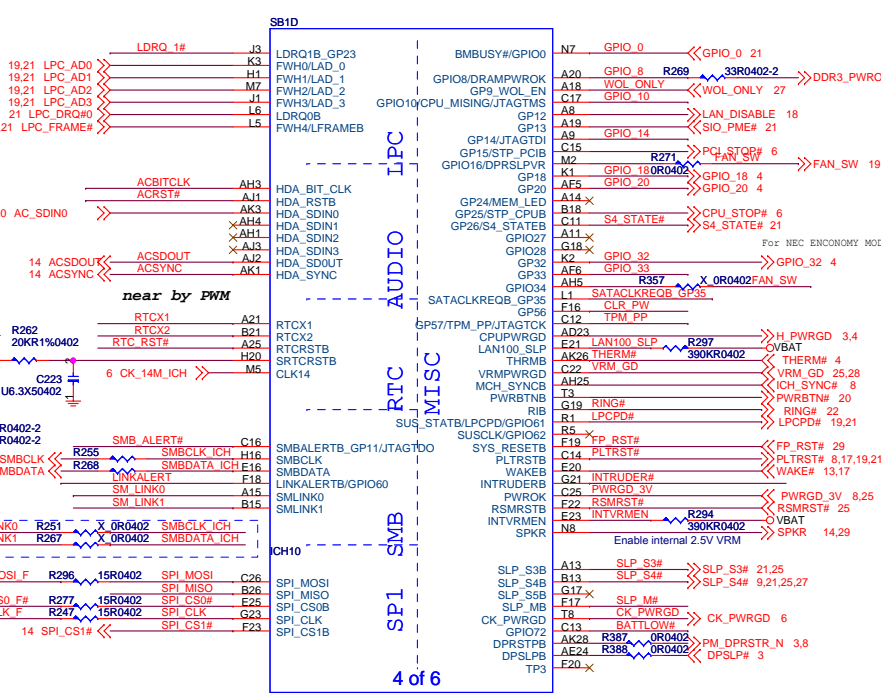
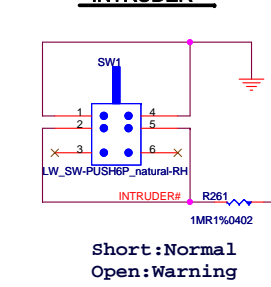


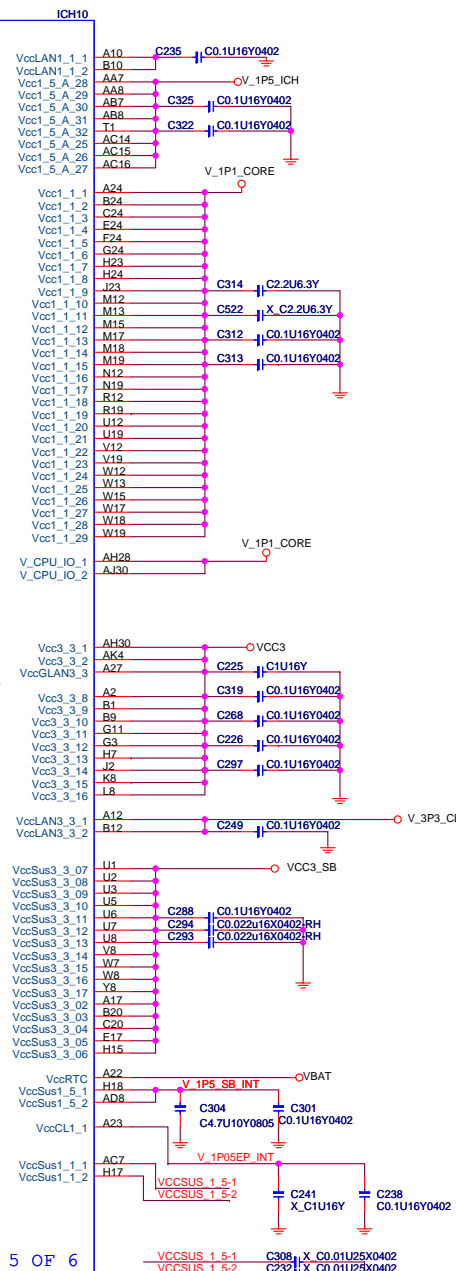
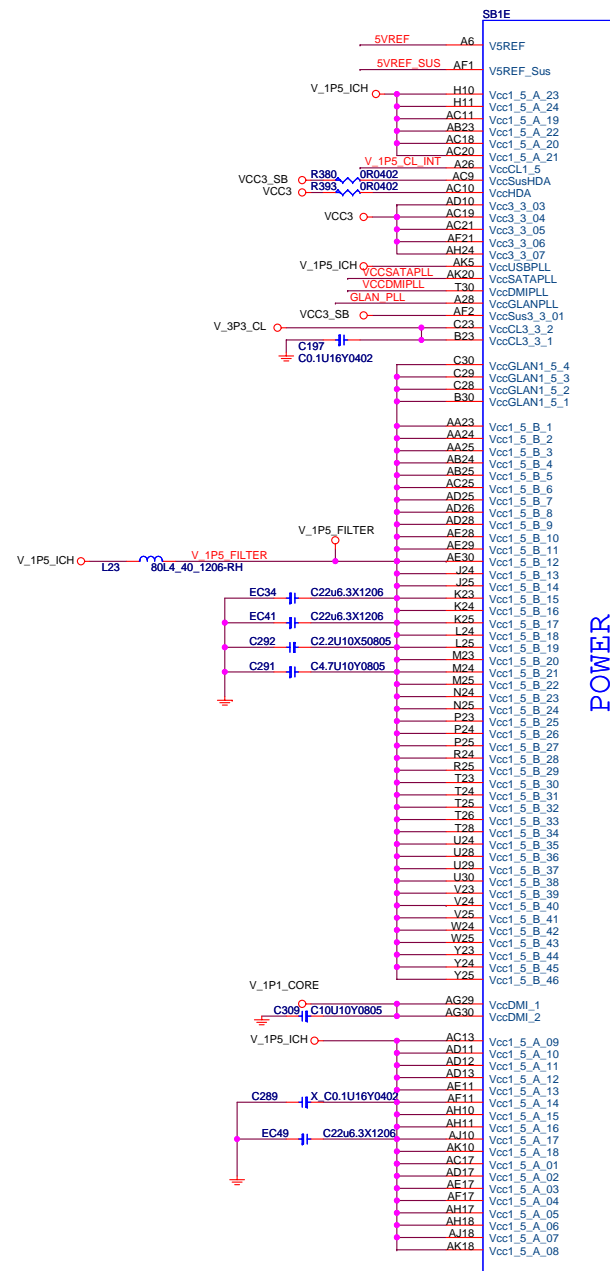
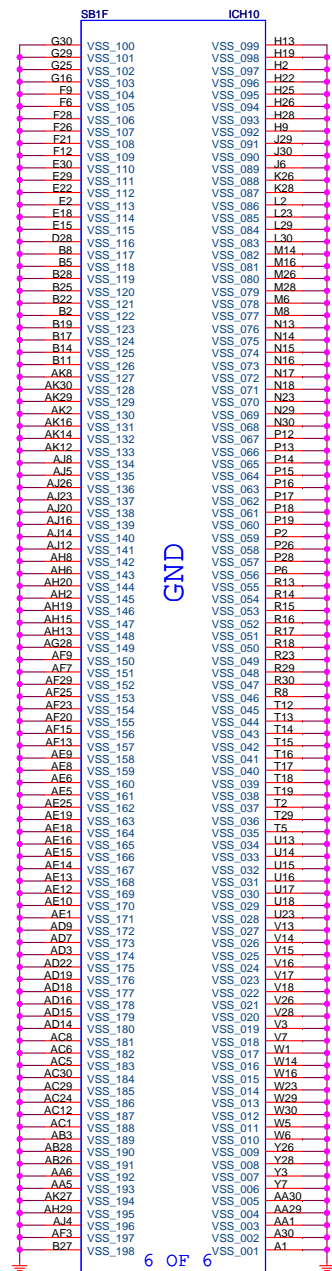
CMOS CLEAR	NORMAL	CLEAR
JBAT1	(1-2)	(2-3)

BATTERY

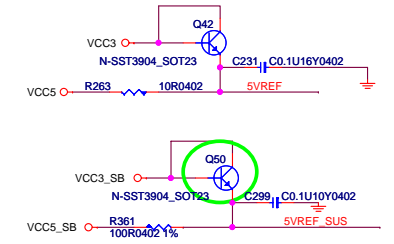


INTRUDER

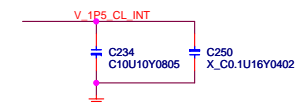




5VREF & 5VREF_SUS Sequencing Circuit



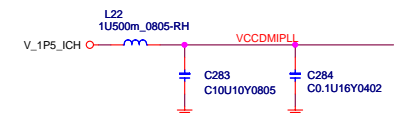
V_1P5_CL decoupling



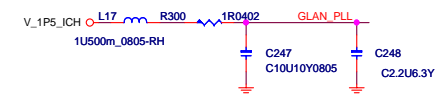
VCCSATAPLL



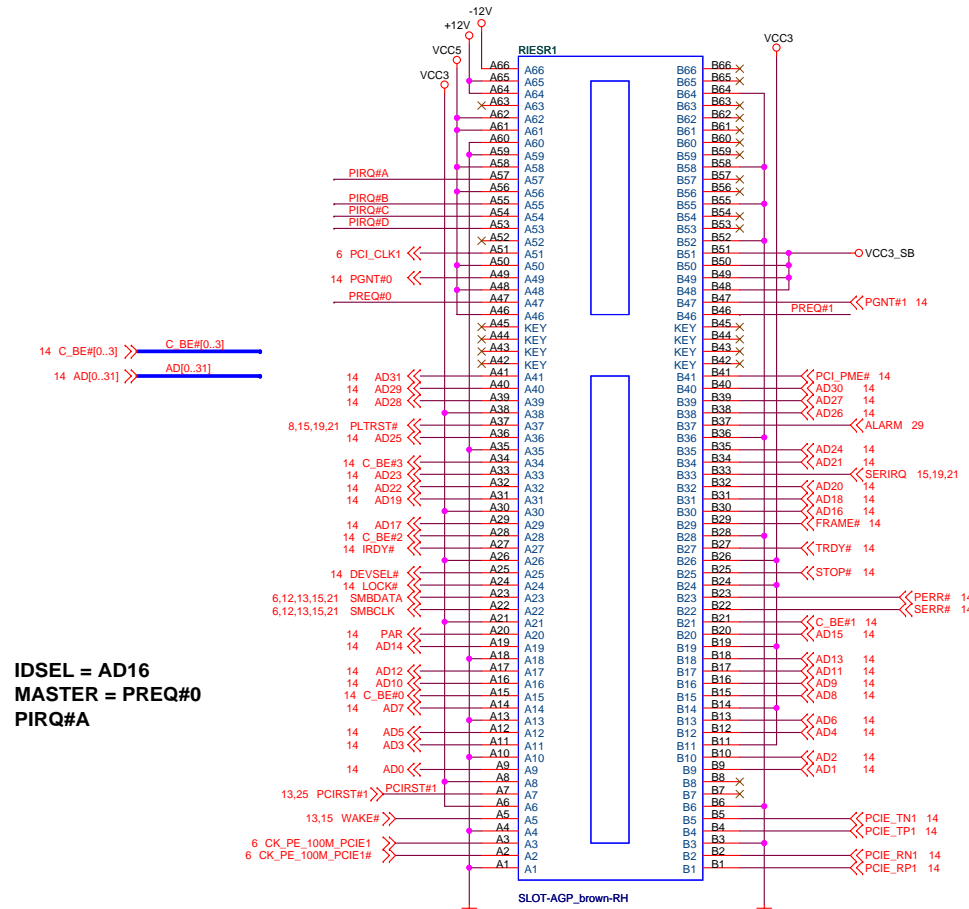
VCCDMIPLL



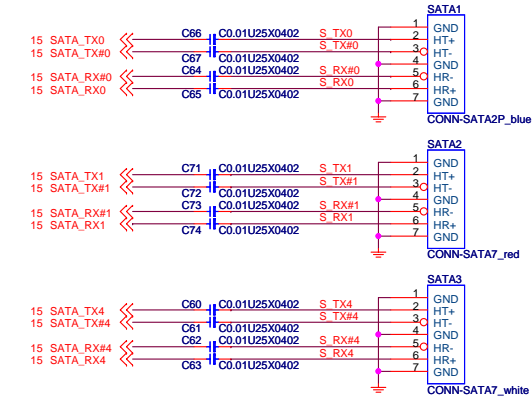
GLAN_PLL



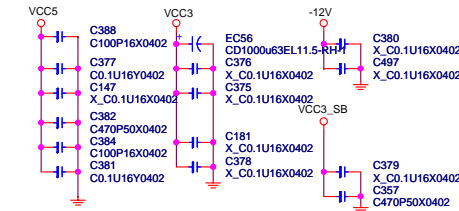
LE riser card interface



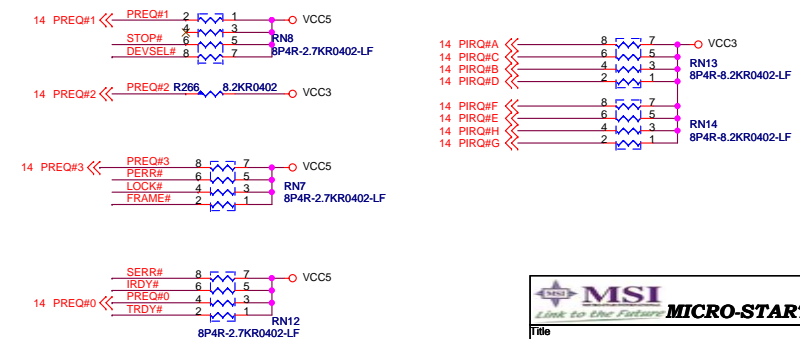
SERIAL ATA CONNECTOR BLOCK



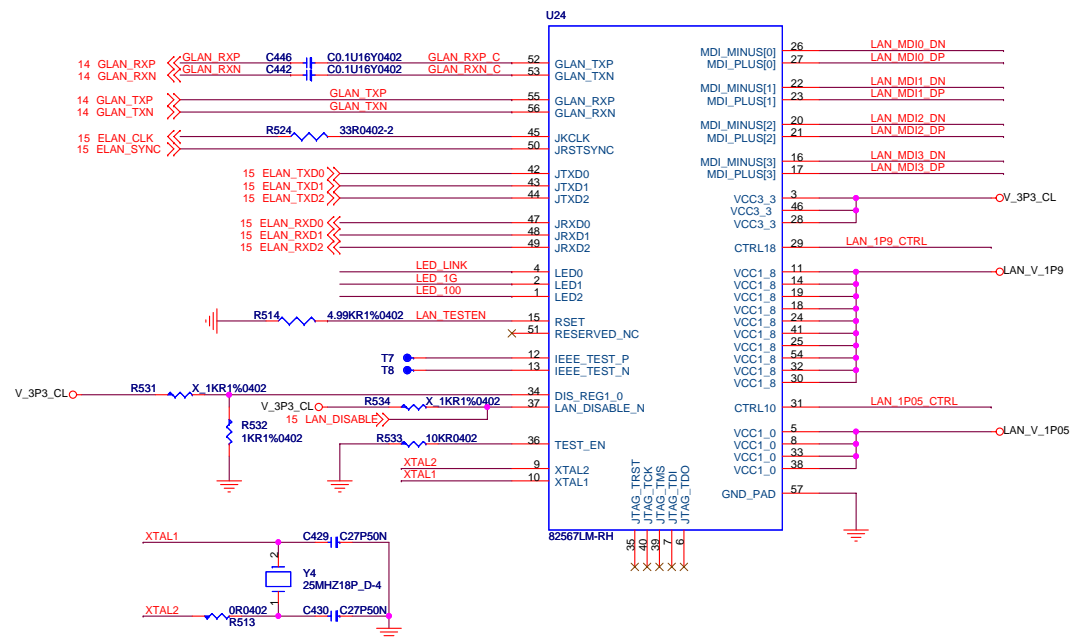
PCI SLOT DECOUPLING CAPACITORS



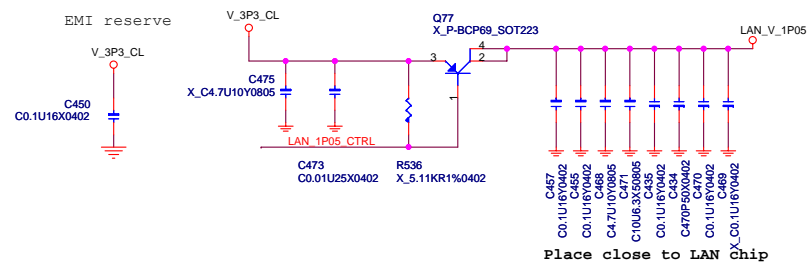
PCI PULL-UP / DOWN RESISTORS



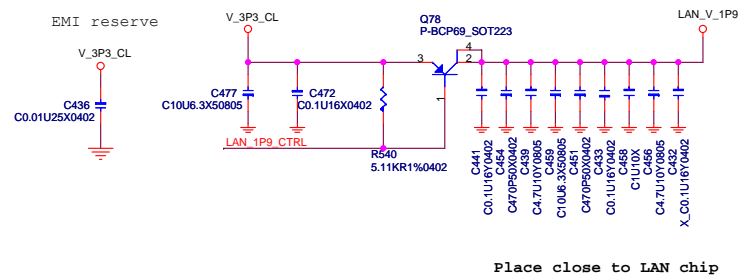
INTEL 82567(Boanman)



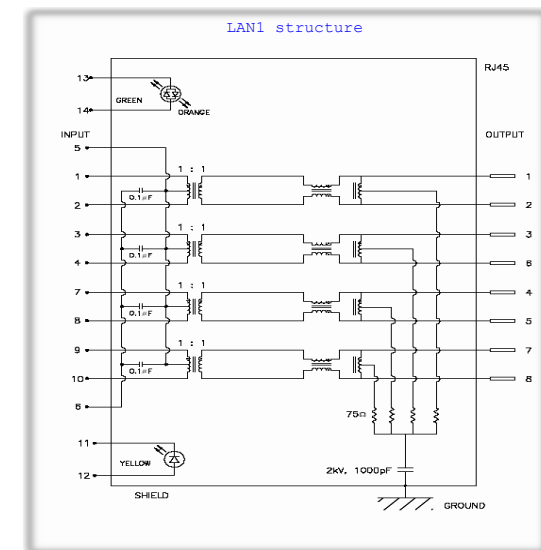
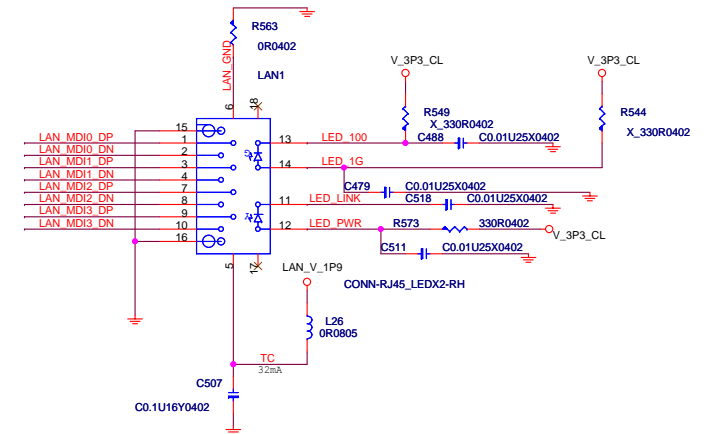
LAN 1P0 POWER
(277.2mA)



LAN 1P8 POWER
(418.2mA)

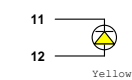
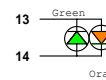


LAN CONNECTOR

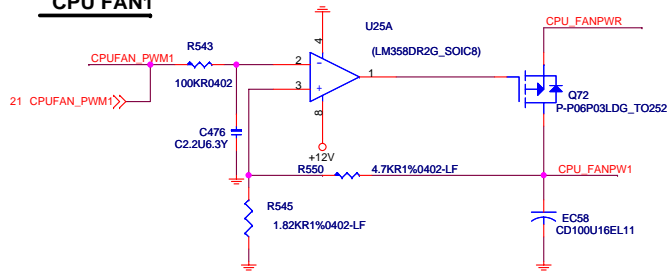


```
Speed LED Type
1000Mbps : Orange
100Mbps  : Green
10Mbps   : LED off
```

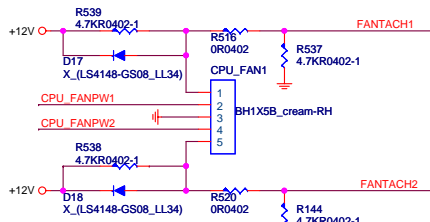
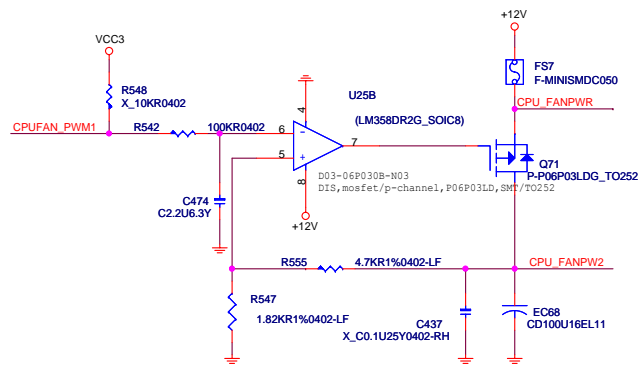
For Active/Link:
Yellow



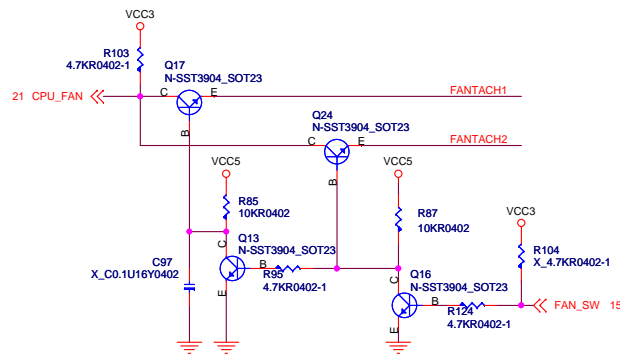
CPU FAN1



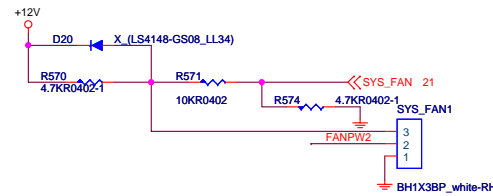
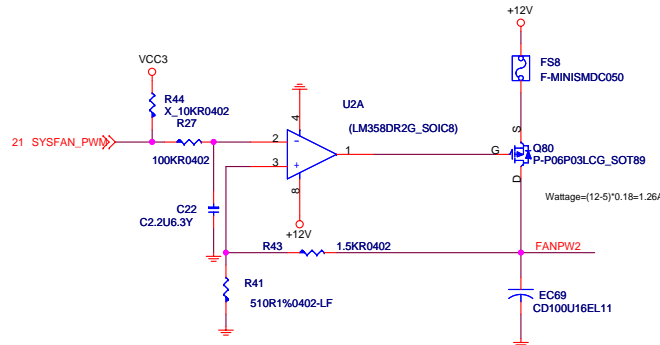
CPU FAN2



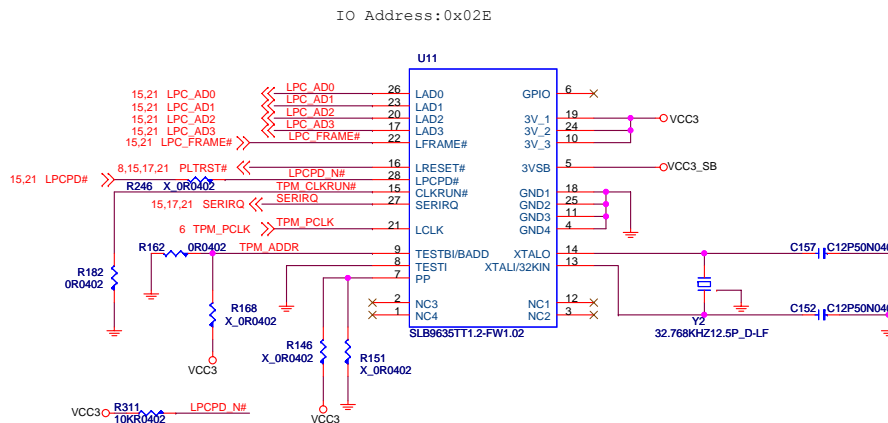
Switch circuit for CPU FAN1&FAN2 detection



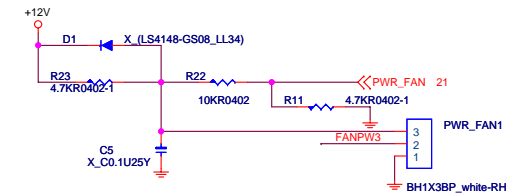
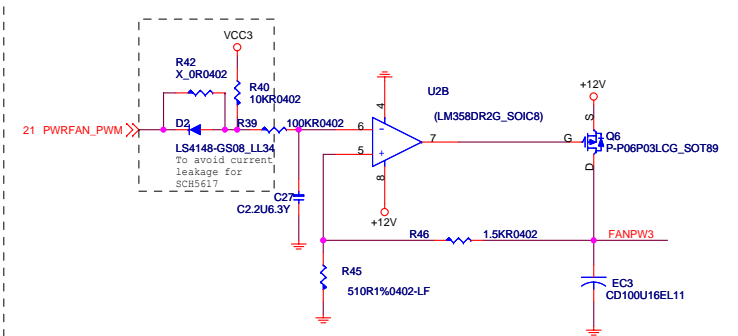
SYS FAN



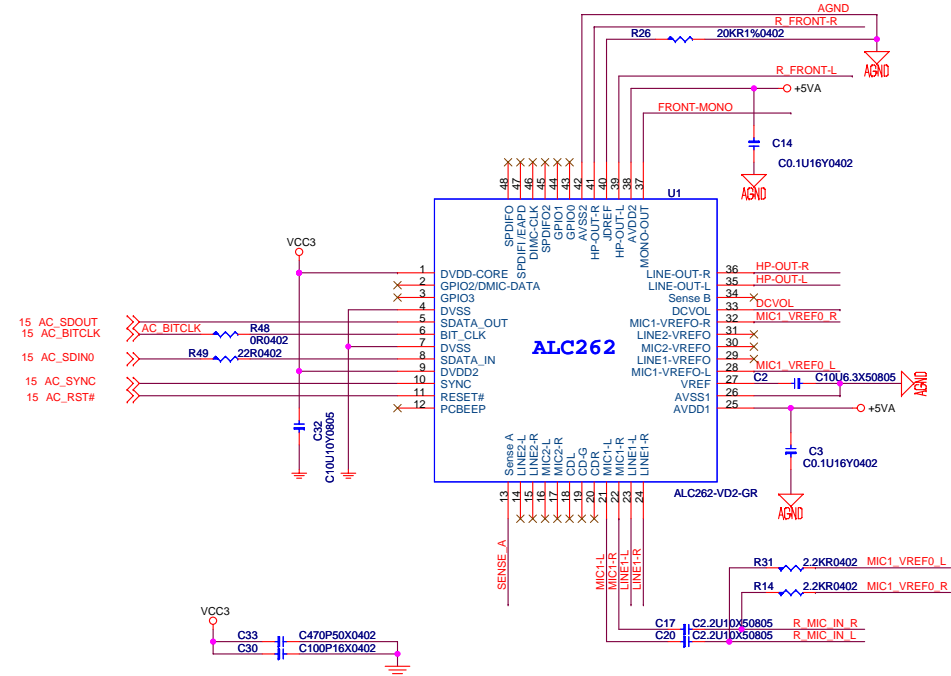
TPM 1.2



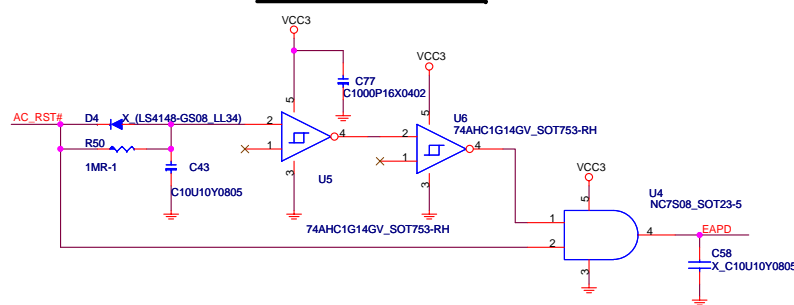
PWR FAN



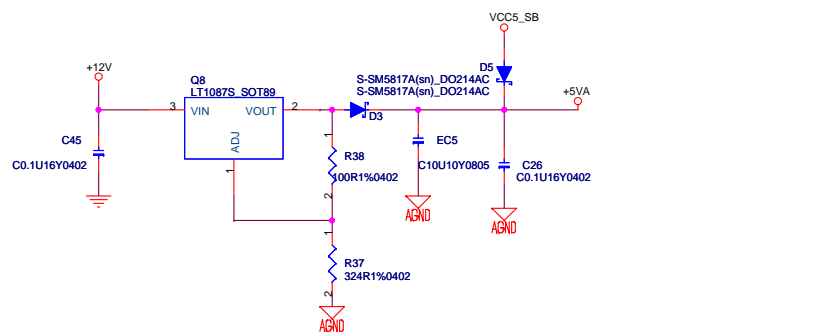
RELTEK HD ALC262VD2



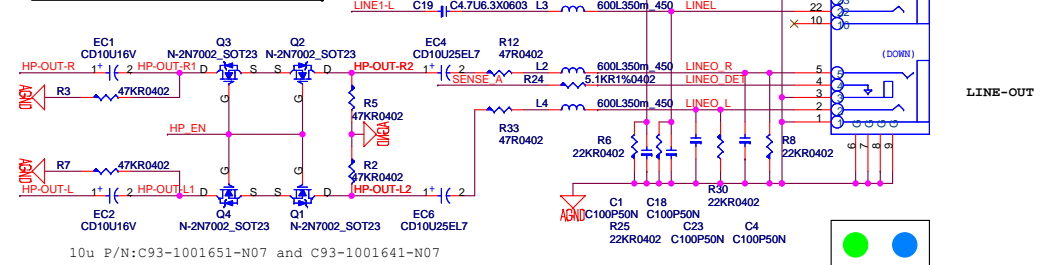
POP noise circuit



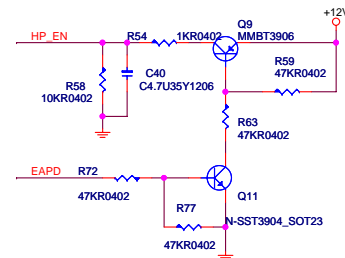
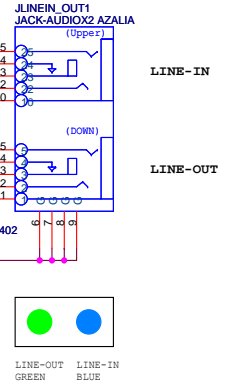
Audio CODEC REGULATOR



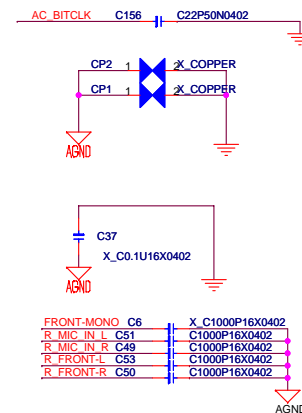
Smooth POP noise circuit



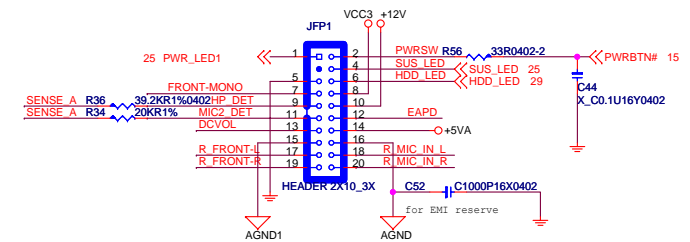
PHONE JACK



For EMI reserve

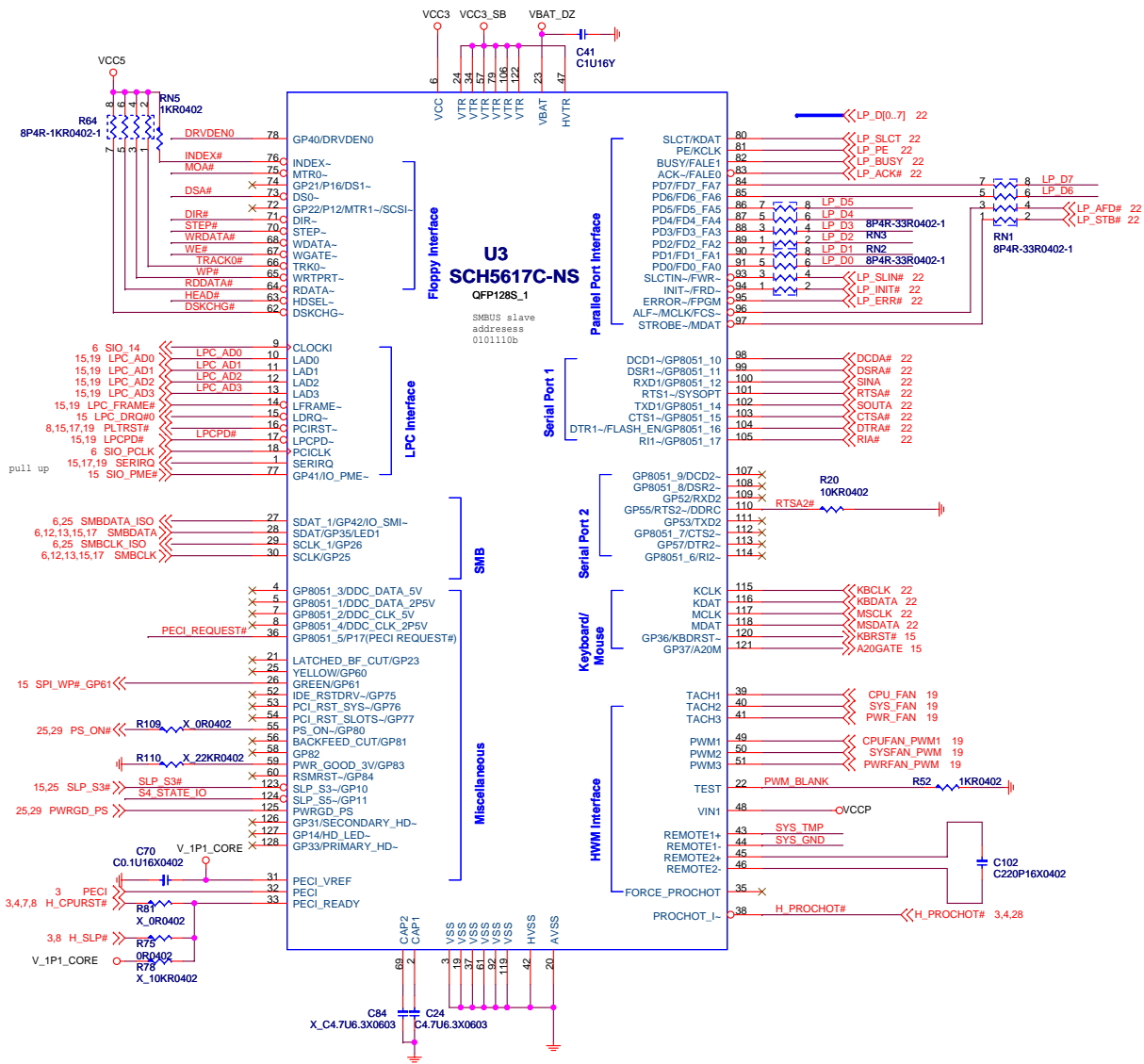


For Front Panel

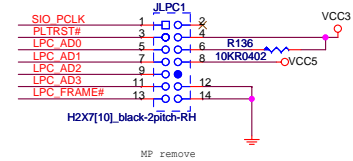


JFP1

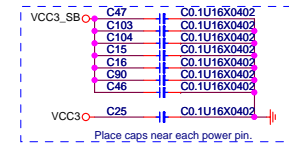
1	PWR_LED	POW_SW	2
3	NC	SLP_LED	4
5	GND	HDD_LED	6
7	Mono	VCC3	8
9	HP_DET	+12V	10
11	MIC_DET	EAPD	12
13	DCVOL	+5VA	14
15	AGND1	AGND	16
17	FRONT_L	MIC_L	18
19	FRONT_R	MIC_R	20



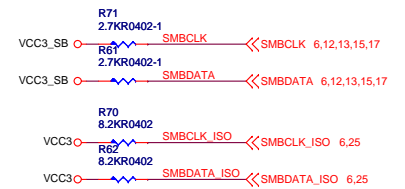
Debug port



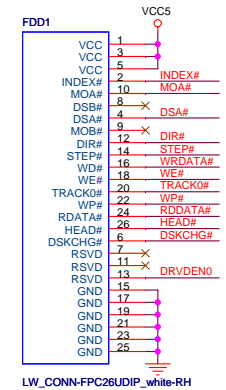
SIO power decoupling



SMBUS pull-up resistor



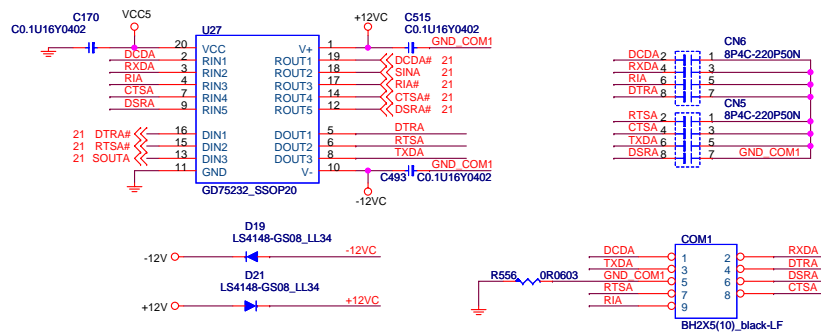
1/2" Notebook type



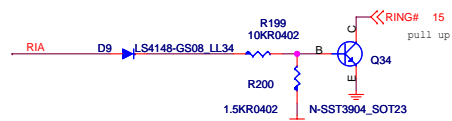
SIO H/W Strap			
Strap	Value	Function	Notes
RTS1#/SYSOPT	0X04E	0X02E	SIO_ADDR
RTS2#/DDRC	READ	READ/WRITE	DDR read/write
DTR1#/FLASH	FLASH	Parallel port	Flash or parallel setup

Flash_EN_Strip:
Should be pulled-down so that the parallel port will work.
DRC Strip:
It's not necessary if don't use DDRC function.

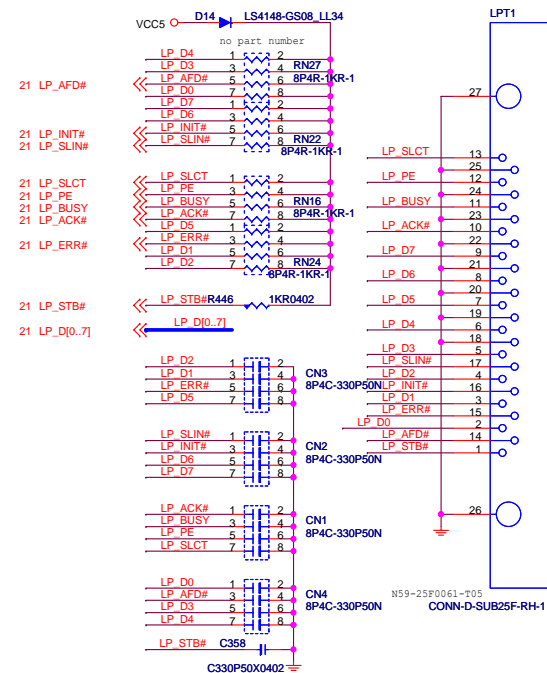
SERIAL PORT 1



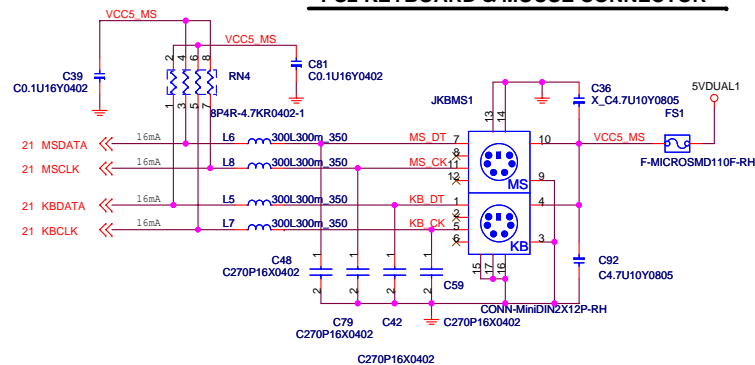
Wake On Modem Header



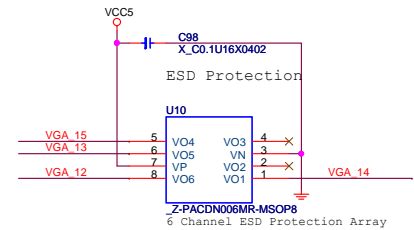
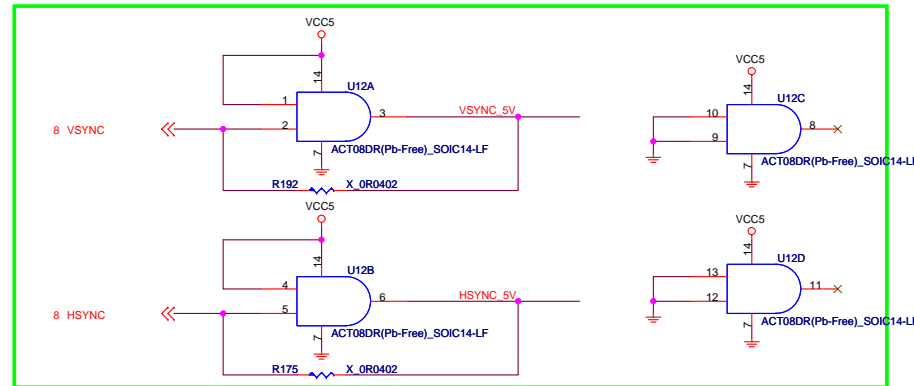
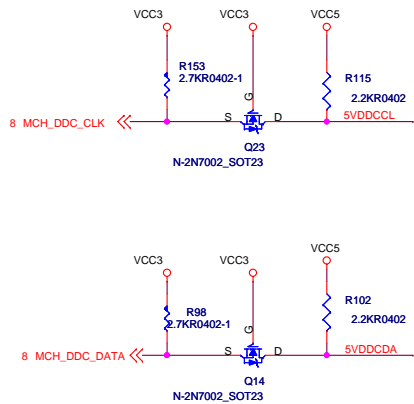
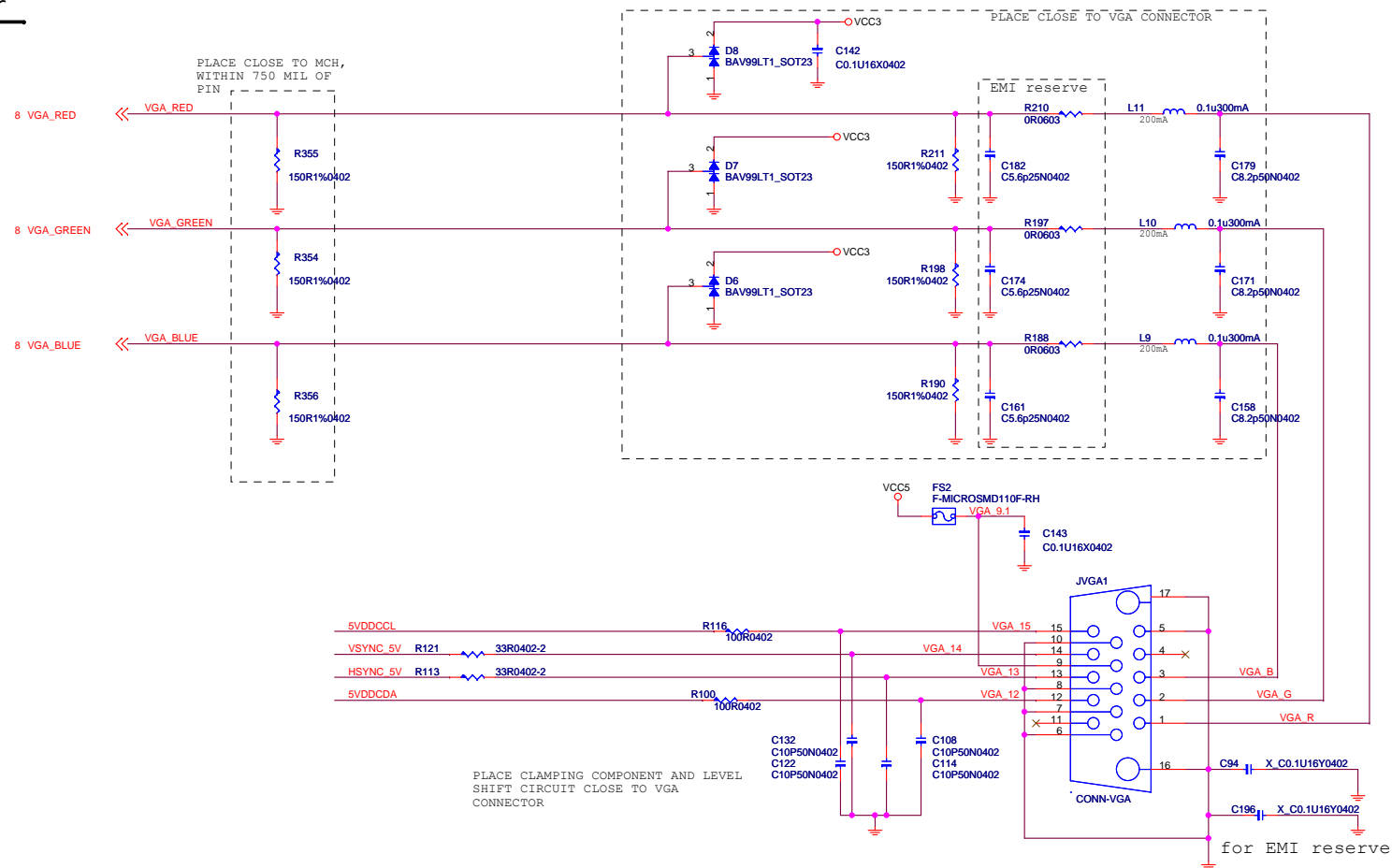
PARALLAL PORT



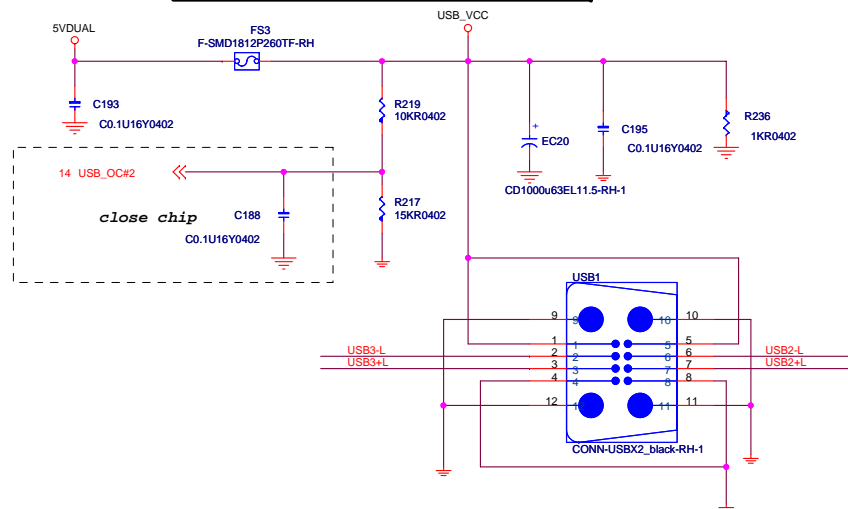
PS2 KEYBOARD & MOUSE CONNECTOR



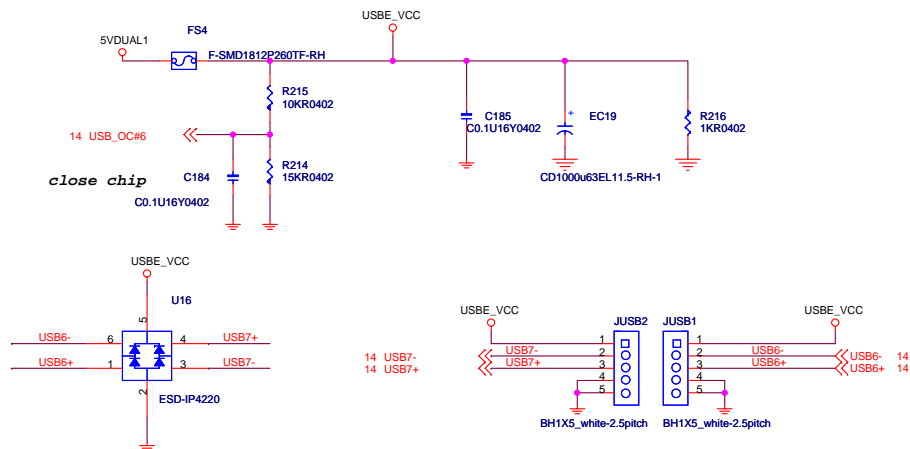
Video Connector



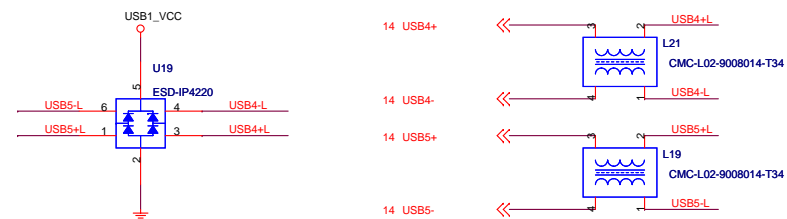
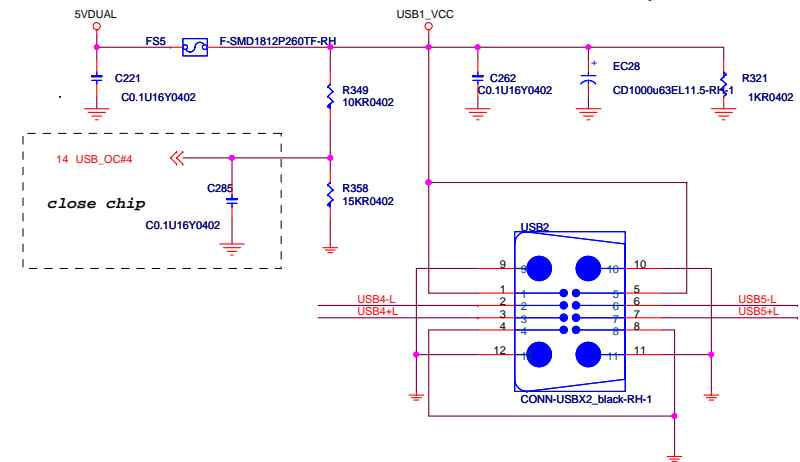
REAR PANEL USB PORT 2,3 CONNECTOR



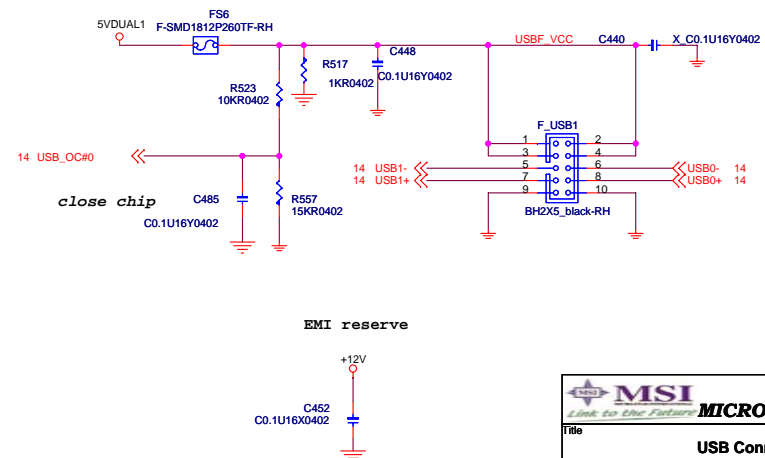
RESERVE EXTERNAL USB PORT 6,7



REAR PANEL USB PORT 4,5 CONNECTOR



FRONT PANEL USB PORT 0,1 CONNECTOR



ACPI Controller

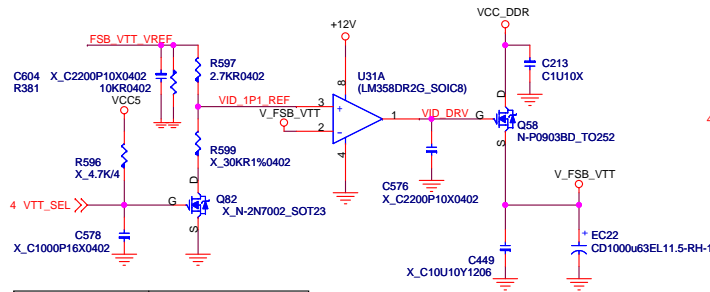
VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

3VSB MODE SELECT

3VSB MODE	5VLDDEC#
SINGLE MOSFET	FULL HIGH
DUAL MOSFET	FULL LOW

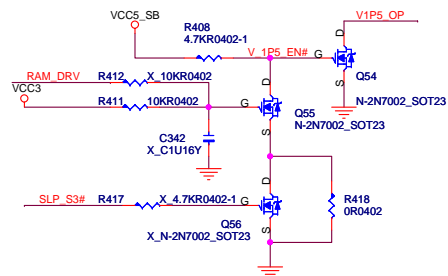
V_FSB_VTT POWER (5.8A) > 4.6A



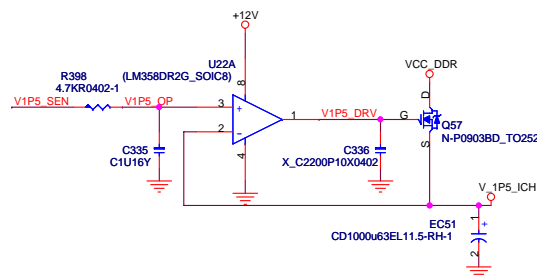
VTT_SEL = H	V_FSB_VTT=1.1V
VTT_SEL = L	V_FSB_VTT=1.2V

INTEL change updated
FSB Vtt will change from 1.1V to 1.2V for All Intel® Series Express Chipsets and the 45nm Intel® Core2 Quad and Intel® Core2 Duo processors.

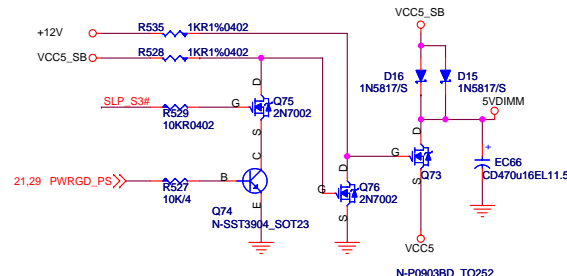
V1P5_SEN S3 power sequency



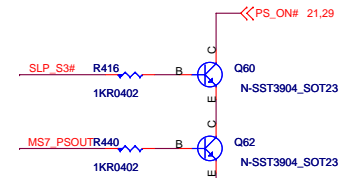
ICH10 1.5V POWER (2.385A)



5VDIMM



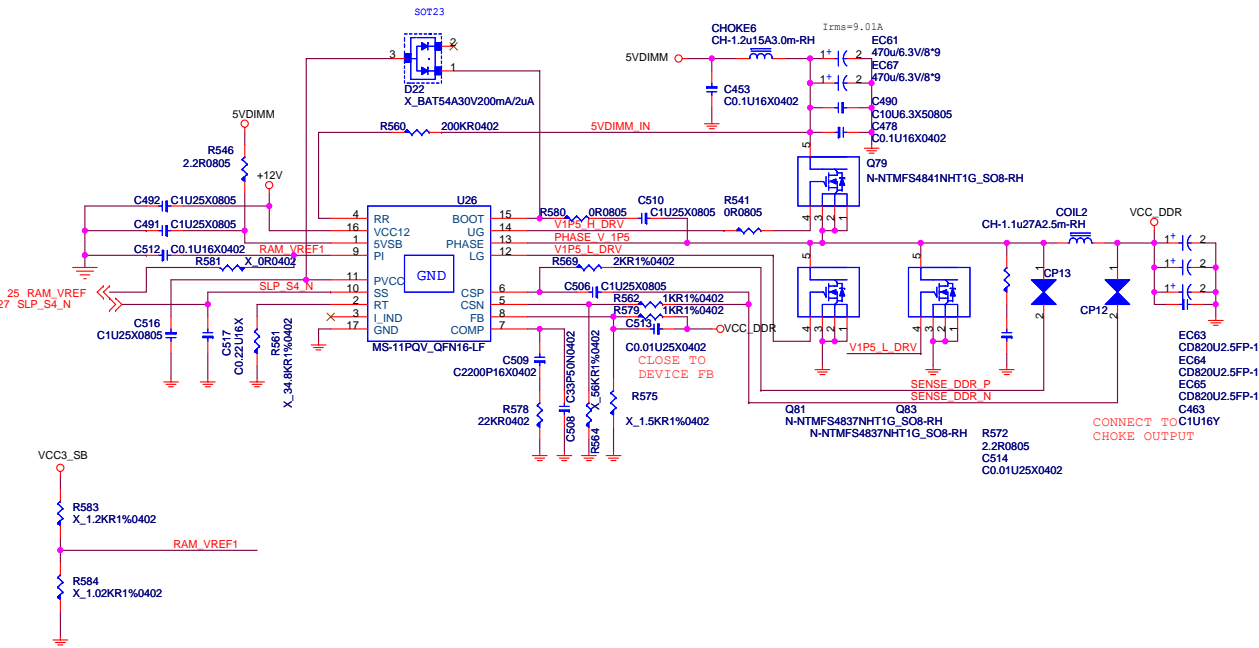
PSON#



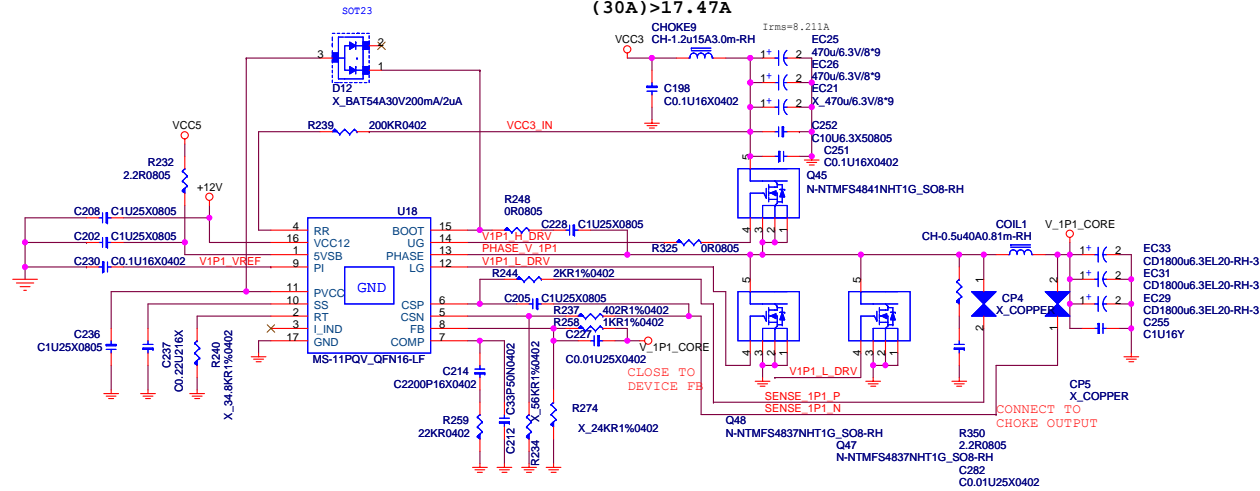
MSI
Link to the Future
MICRO-START INTL CO.,LTD.

ACPI CONTROLLER MS7		
Size	Document Number	Rev
	MS-7420N1	0D
Date:	Wednesday, June 25, 2008	Sheet 25 of 35

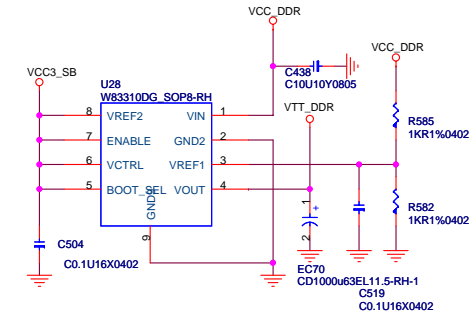
DDRIII 1.5V POWER
(24.89A) > 19.66A



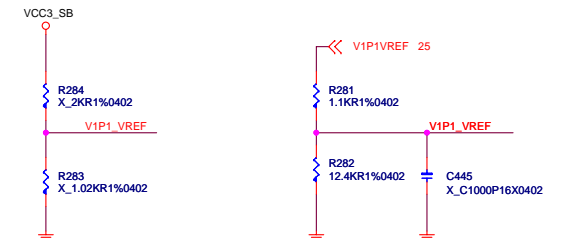
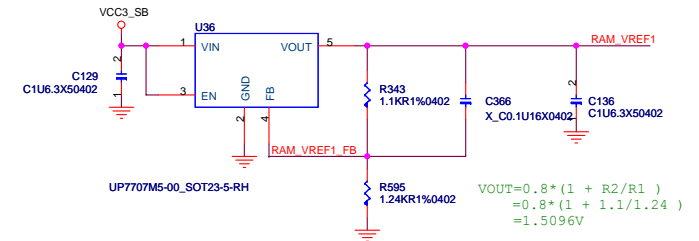
GMCH/ICH10 1.1V POWER
(30A)>17.47A

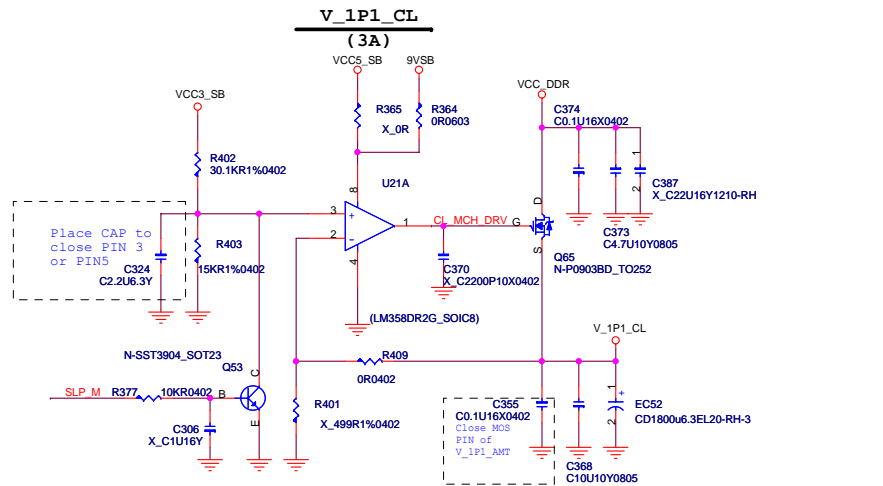


DDR VTT Power
(0.83A)

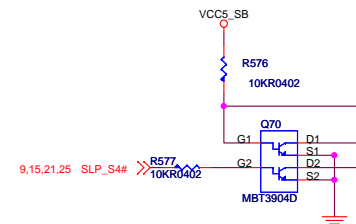


VCC_DDR reference Power

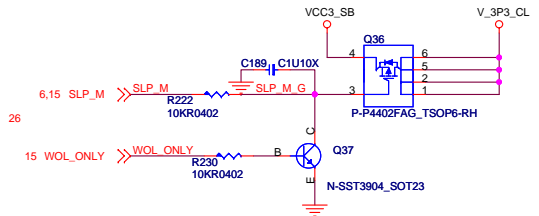




DIMM Softsart for iAMT

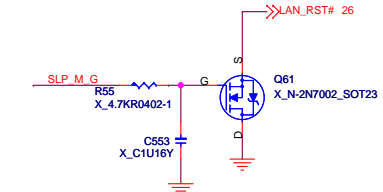


V_3P3_CL (711mA)

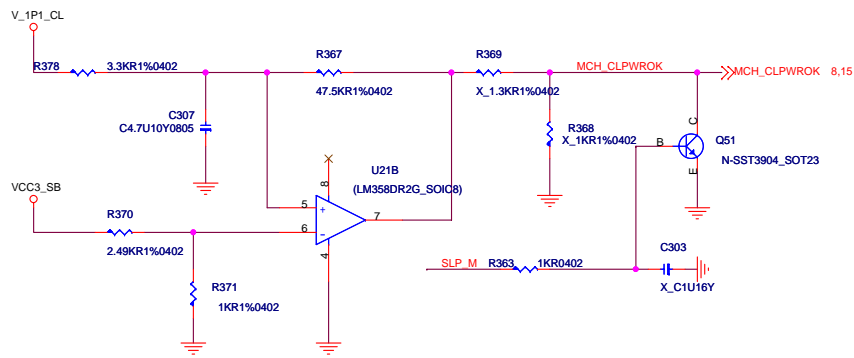


LAN_RST# PATCH

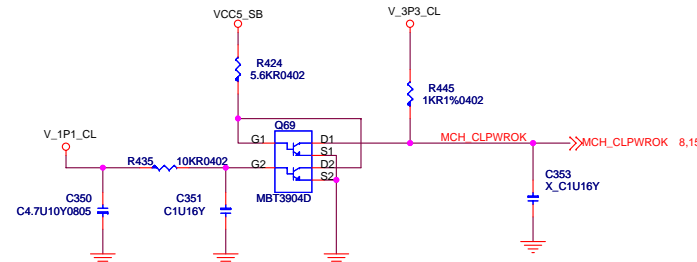
Accordng to INTEL MOW23



Reserve CL_PWROK circuit

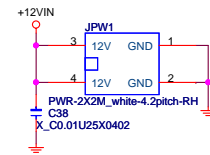
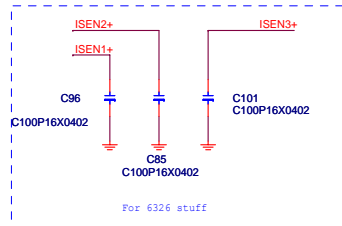
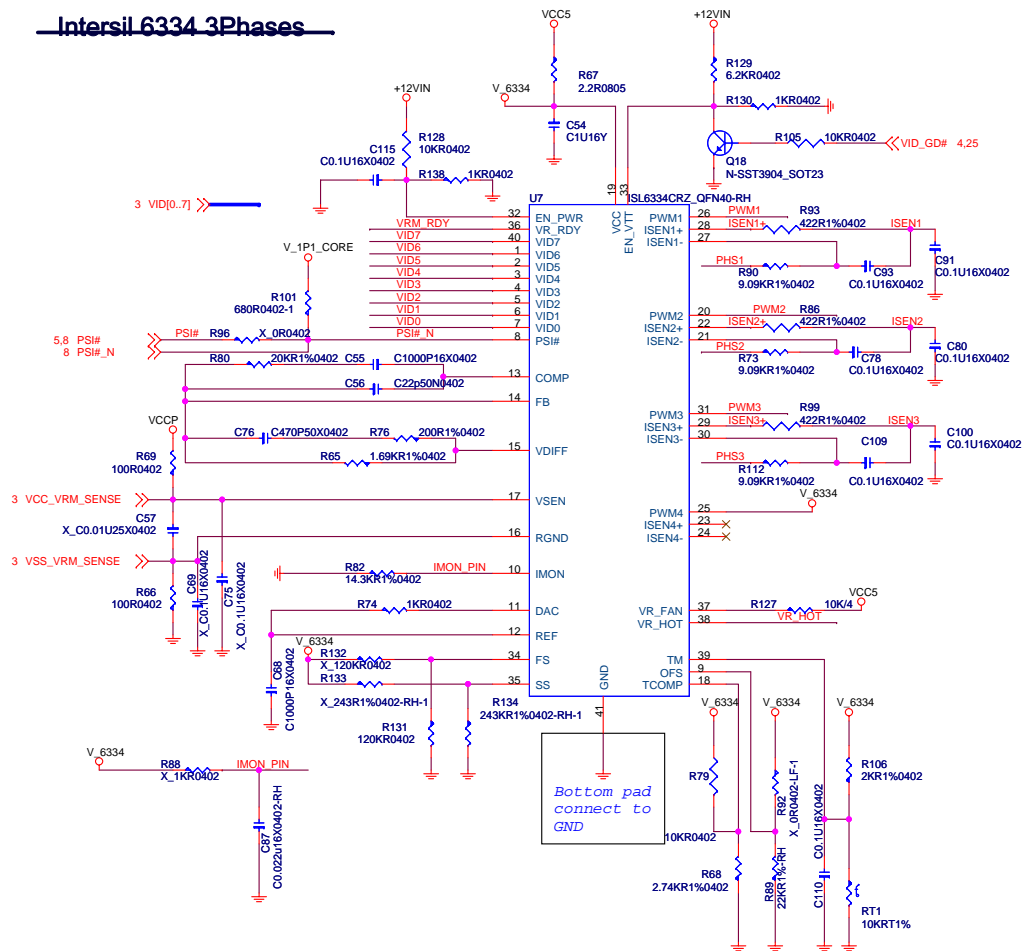


CL_PWROK



Note:
 SLP_S4#
 AMT Disable-->indicate ACPI S4 state,DRAM power off.
 AMT Enable-->not be asserted ACPI S4 state,DRAM power ON
 SLP_M#
 AMT Enable SLP_M#-->Control the overall power to Intel AMT during ACPI S3-S5.
 S4_SATE#
 AMT Enable-->indication of ACPI S4 state

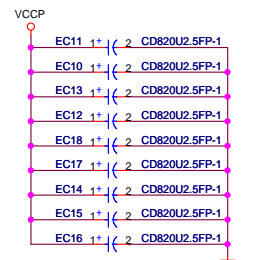
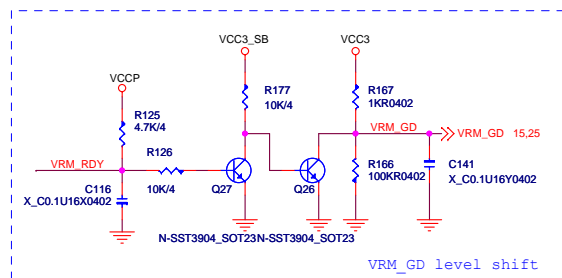
Intersil 6334 3Phases



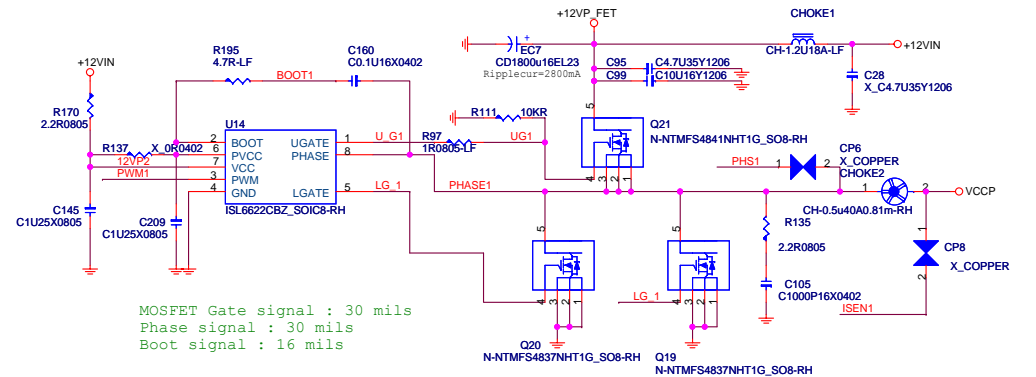
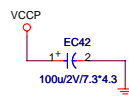
TDK
NTCG104KF104FT

```
VR FAN TRIP:1.69V ~ 80 degC
VR HOT TRIP:1.44V ~ 90 degC
```

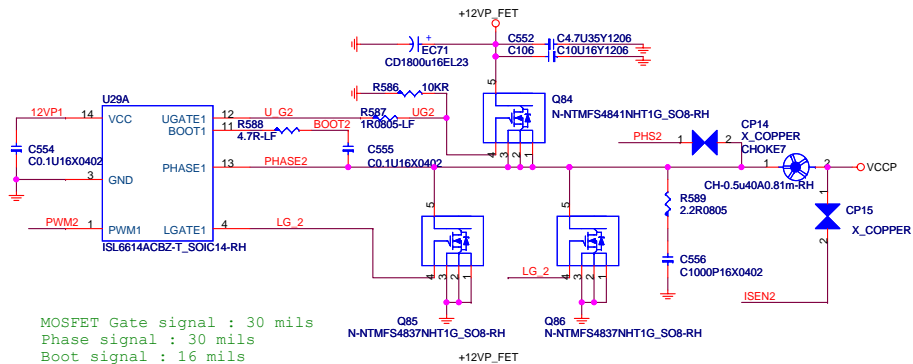
OS-CON Capacitors



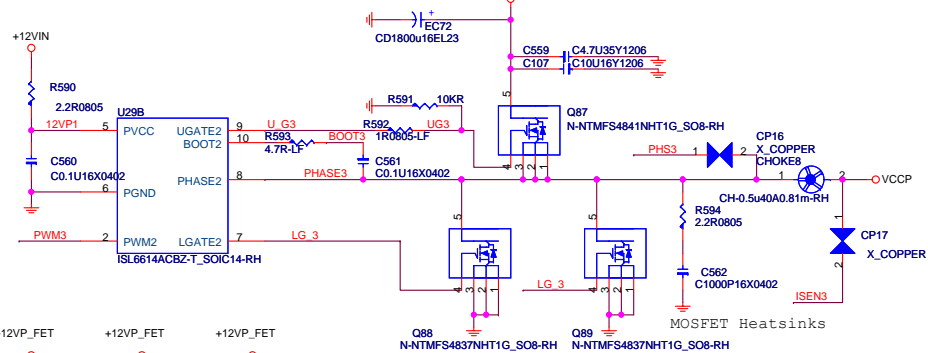
SP Capacitors



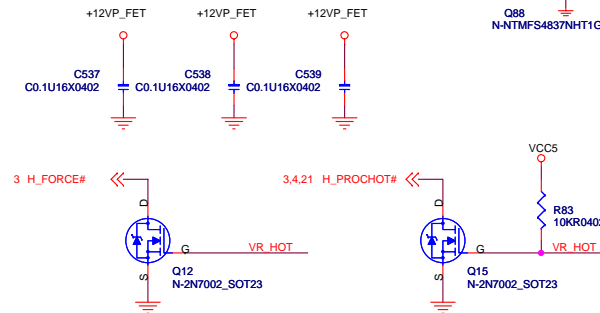
```
MOSFET Gate signal : 30 mils
Phase signal : 30 mils
Boot signal : 16 mils
```



```
MOSFET Gate signal : 30 mils
Phase signal : 30 mils
Boot signal : 16 mils
```



MOSFET Heatsinks



15 SATELA#

VCC5

R57 1KR0402

Q10

R53

4.7KR0402-1

P-MMBT390LT1G_SOT23-RH

Ic=200mA
Vbe=5V
Vceo=40V

120R

R142

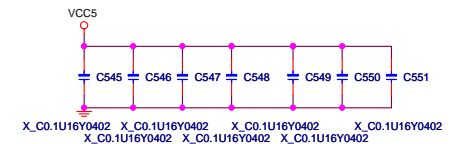
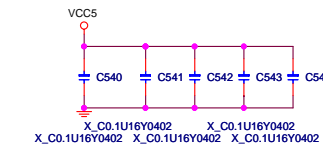
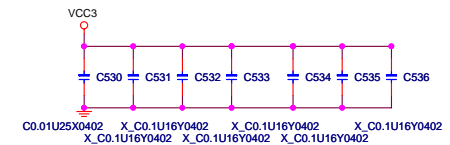
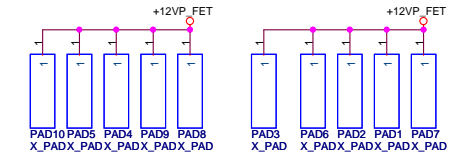
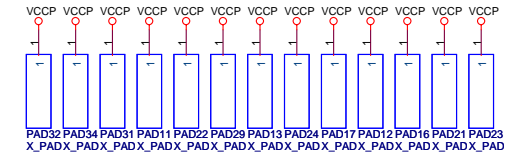
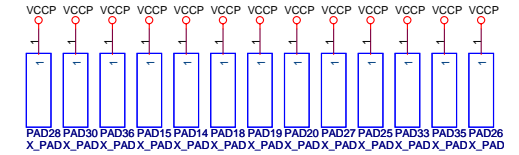
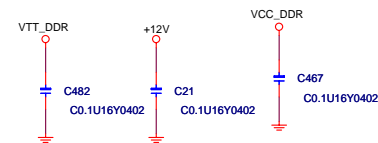
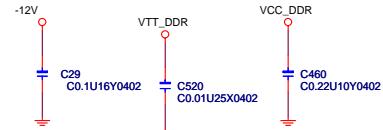
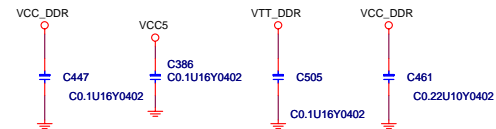
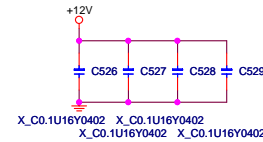
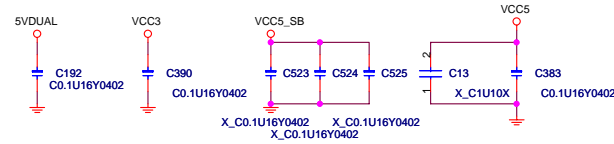
<<< SATELA#

<<< HDD_LED 20

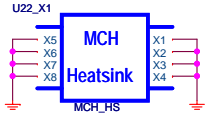
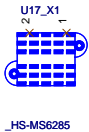
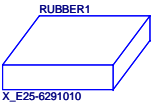
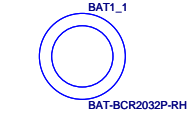
C199 C0.1U16Y0402

Place near CK_48M_USB_ICh for EMI.

V_1P1_CORE
C305 C0.1U16Y040
Place near R643 for EMI.



Auto-BOM Manual Parts



ICH10

GPIO Pin	Type	Default	Function	Power	MUXED / UNMUXED	Pin-out
GPIO 0	I/O	GPI	BMBUSY# function, Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	Reserve for DDR_PEROK, Pull-up to VCC_DDR with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	LAN_DISABLE	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	SIO_PME# connect to SIO, pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# for CK505 IAMT	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	FAN switch, pull-up VCC3 with 10K.	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull-up VCC3 with 10K(Not Use)	VCC3	MUXED	J3
GPIO 24	I/O	NC		3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# for CK505 IAMT	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE#	3.3V_SB		C11
GPIO 27	I/O	GPO	NC	3.3V_SB		A11
GPIO 28	I/O	GPO	NC	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#6 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#6 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	PROHOT# for NEC Economy mode	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	Pull-up to VCC3 with 4.7K through JC11 Jumper. (Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	NC	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	Clear password	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#6 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#6 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping, pull-down 2.2K to GND	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#	VCC5	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3# (Not Use)	VCC3	MUXED	F7
GPIO 56	I/O	GPI	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to VCC3_SB with 10K directly for TPM_PP	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS# (Not Use), SPI_CS1_F# (Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Riser slot (PCI1)	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDR2 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A2/SCLK_A2#
DIMM 2	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#

SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP41	77	SIO_PME#	OUTPUT
GP25	30	SMBCLK	INPUT
GP26	29	SMBCLK_ISO	INPUT
GP35	28	SMBDATA	OUTPUT
GP42	27	SMBDATA_ISO	OUTPUT

SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH10, PCI EXPRESS[X16][X1]
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JC11	(1-2)Normal	(2-3)ME Disable for FPROG
J1	(1-2)short: Normal	(1-2)Open: Clear PW

LGA775-CPU		
0.8375V - 1.6000V Core	-	84A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.33A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.3A

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Boazman GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6334		
VCCP VRD11.1	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

MS11+ SW-Power		
VCC_DDR	-	1.5V PWM 19.66A

MS11+ SW-Power		
V_1P1_CORE	-	1.1V PWM 17.47A

MS7 Controller		
V_1P1_CL	-	1.1V Linear 3A

V_1P5_ICH		
1.5V Linear	-	2.385A

VCC3_SB		
3.3V Linear	-	3.96A

5VDUAL1		
5V Switch	-	4.367A
5VDIMM		
5V Switch	-	8.29A

DDRIII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	3.6A
1.5V VCC_DDR (S3)	-	TBDmA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

AGP Extender riser slot		
	Luner Eagle	
+12V	-	1A
+5V	-	5.0A
+3.3Vaux	-	750mA
+3.3V	-	10.6A

PCI_E x1 slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	3.0A

PCI slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	7.6A
+5V	-	5.0A

USB x 8		
+5V (S0,S1)	-	4A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

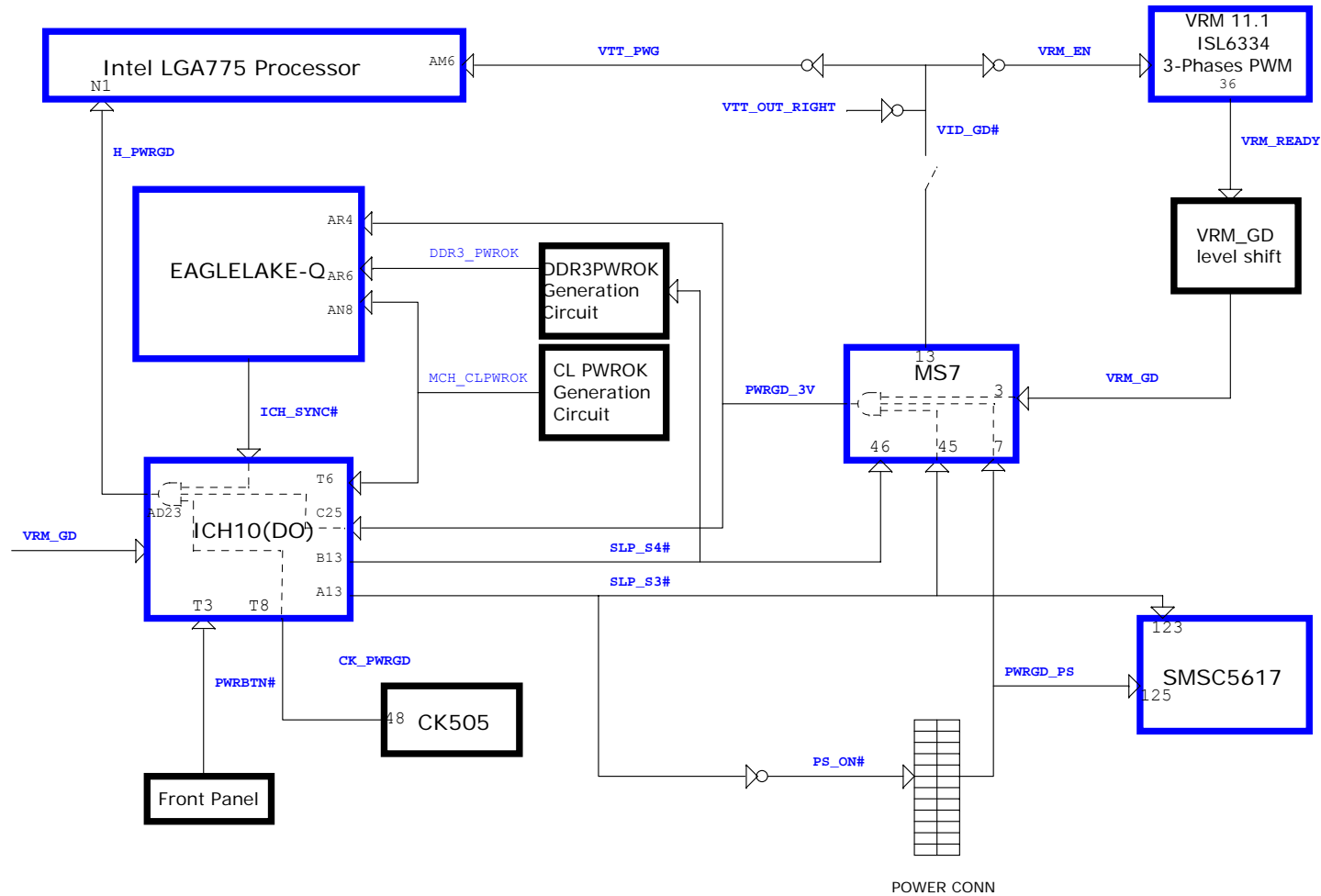
5VAudio
+5VR
500mA

3V
Battery

+12V
ATX
2x2

+5V +3.3V +5VSB +12V
ATX POWER

PWROK MAP



[illegible]

76Add V_FSB_VTT circuit and change capacitor of related with V_FSB_VTT to 1.2V.....Intel design change update..
77Add Q83.....Due to V_FSB_VTT become to 1.2V ,VTT_DDR POWER increase to 19.66 A, so add a low size MOS for DDR POWER.
78Remove EC72.....Due to V_FSB_VTT become to 1.2V ,V_1P1_CORE reduce from 23.27 A to 17.47 A,I rip become to 8.211A,so remove EC27.
79..Reserve R84,R91,R94,R413 between V_FSB_VTT and V_1P1_CORE.....
80Use copper instead R311Due to V_FSB_VTT become to 1.2V for layout space concern.
81Delete R399.....Have not use.
82Stuff R55,R246 un-mount.....For INFINEON require, change LPCPD# of TPM 1.2 to VCC3